CONTROL DATA CORPORATION

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ENHANCED SMALL DEVICE INTERFACE SPECIFICATION

MAGNETIC PERIPHERALS, INC.
a Control Data Company

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ENHANCED SMALL DEVICE INTERFACE

SPECIFICATION

REVISION D1

November 28, 1984

ENHANCED SMALL DEVICE INTERFACE

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ENHANCED SMALL DEVICE INTERFACE

1.0 SCOPE

This document defines the Enhanced Small Device Interface (ESDI) specification. It represents the merging of the the Enhanced Small Disk Interface specification and the Enhanced Small Tape Interface specification.

The general portions covering electrical and physical interfacing can be found in sections 2.0 through 4.0. Specific information concerning interfacing of disk drives can be found in Section 5.0 (Serial mode implementation) and Section 6.0 (Step mode implementation) while specific information concerning the interfacing of tape drives can be found in Section 7.0. Either Section 5.0, 6.0, or 7.0 may be implemented independently of the other or combined if so desired.

The primary objectives in developing this specifications was to:

(1) provide a low cost, high performance interface definition suitable for the smaller, high performance memory devices currently being produced,

(2) develop a standard which could support higher data transfer rates as well as provide for additional performance features that are desireable on higher performance systems.

(3) provide a single interface definition which could effectively support both disk and tape drives on the same controller.

In order to accommodate a number of product types, the specification defines several alternatives.

For the disk portion, two implementations are possible: Serial (Section 5.0) and Step (Section 6.0).

The Serial mode of operation utilizes NRZ data transfer along with serial commands and serial configuration and status reporting across the command cable (J1).

The Step mode implementation utilizes the same NRZ data transfer; however, the STEP and DIRECTION lines are used to cause actuator motion. Hence, configuration and status reporting are unavailable over the interface.

This specification does not require that both of these modes be available on any drive; rather, it is the choice of the disk drive manufacturer which mode to implement. If desired, both modes may be offered with a selection method provided by the manufacturer.

COMMENTS

This specification describes the Industry Standard ESDI (Enhanced Small Disk Interface) and is reproduced in it's original form as developed by the ESDI Committee.

Reference by Control Data to the ESDI specifies the parameters outlined in this document. CDC Products supporting the ESDI are designed to this specification. Any variation from this specification by a CDC ESDI Product will be noted in detail by the respective Product Specification.

Section 7.0 of the specification provides for the attachment of either streaming or start/stop tape drives to the same ESDI controller. Because of the characteristics of tape devices, only a serial mode of implementation is supported.

Both the physical and logical interface characteristics of tape and disk drives have been included in these specifications. Certain design considerations were made to allow optimized operation of the disk drive with a tape device. For exmaple, simultaneous disk and tape access is possible allowing direct disk-to-tape transfers to occur without host intervention. Provision for multiple radial data channels has been provided to enhance the intra-device data transfer rates. This specification supports cable lengths of up to three meters (9.8 feet).

2.0 GENERAL DESCRIPTION

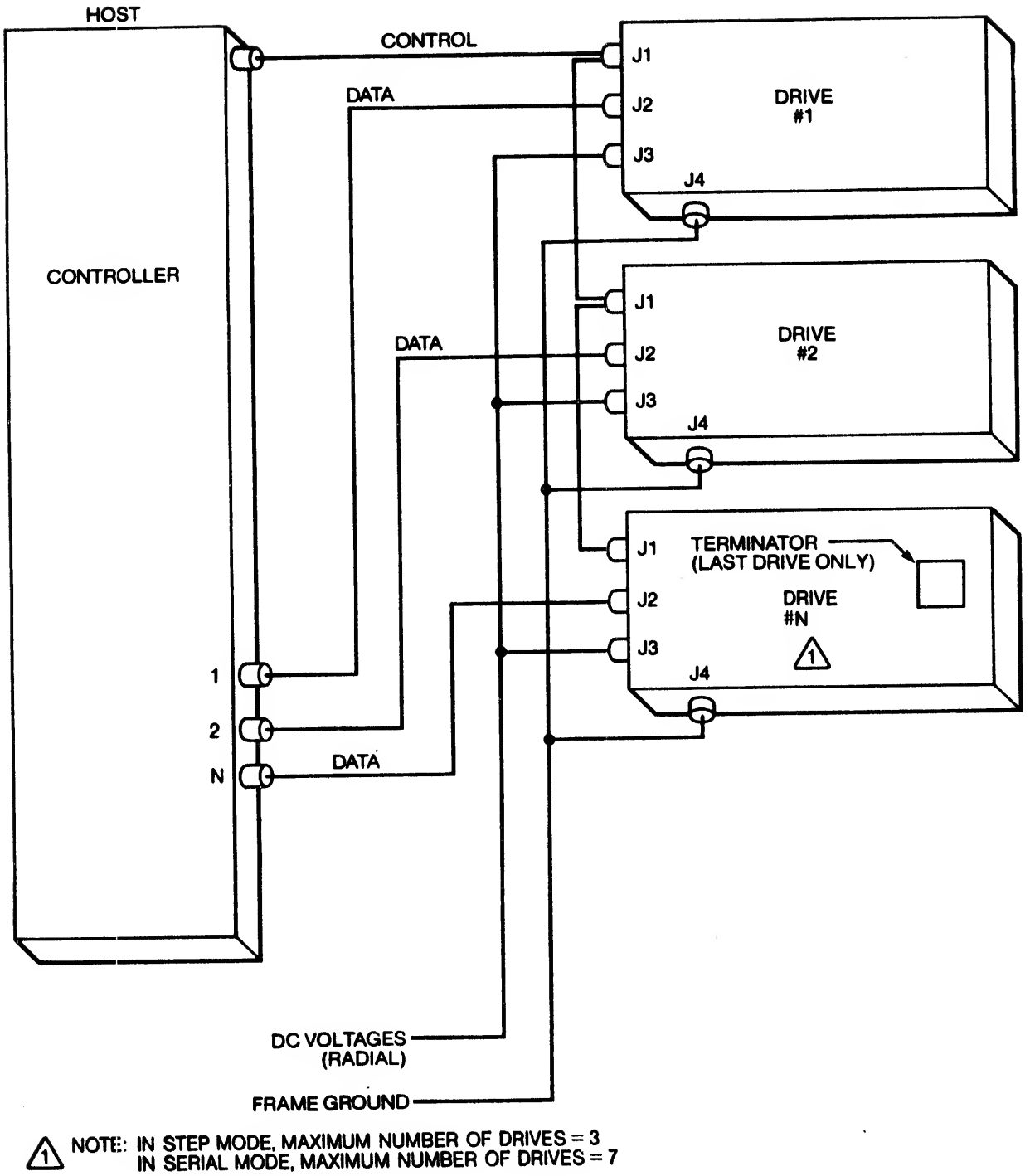
The Enhanced Small Device Interface consists of a control cable and a data cable. The control cable allows for a daisy chain connection of up to three disk drives (in STEP mode) and up to seven disk and tape drives (in SERIAL mode) with only the last drive being terminated. See Figure 1. The data cable must be attached in a radial configuration.

3.0 ELECTRICAL INTERFACE

The Enhanced Small Device Interface can be divided into three categories, each of which is physically separated.

1. Control signals.
2. Data signals
3. DC power.

All control lines are digital in nature (open collector TTL) and either provide signals to the drive (input) or signals to the host (output). The data transfer signals are differential in nature and provide data either to (write) or from (read) the drive.



1 NOTE: IN STEP MODE, MAXIMUM NUMBER OF DRIVES = 3
IN SERIAL MODE, MAXIMUM NUMBER OF DRIVES = 7

E-101-0

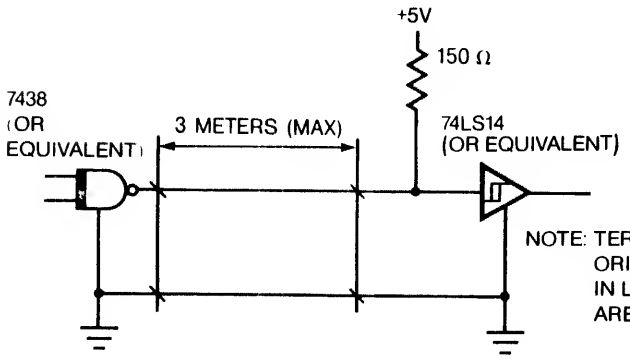
TYPICAL CONNECTION, MULTIPLE DRIVE SYSTEM
FIGURE 1

3.1 Control Signal Drivers and Receivers

The drivers have the following electrical specifications. Refer to Figure 2 for the recommended circuit.

TRUE/ACTIVE: 0.0 VDC to 0.4 VDC @ I= -48mA (Max)

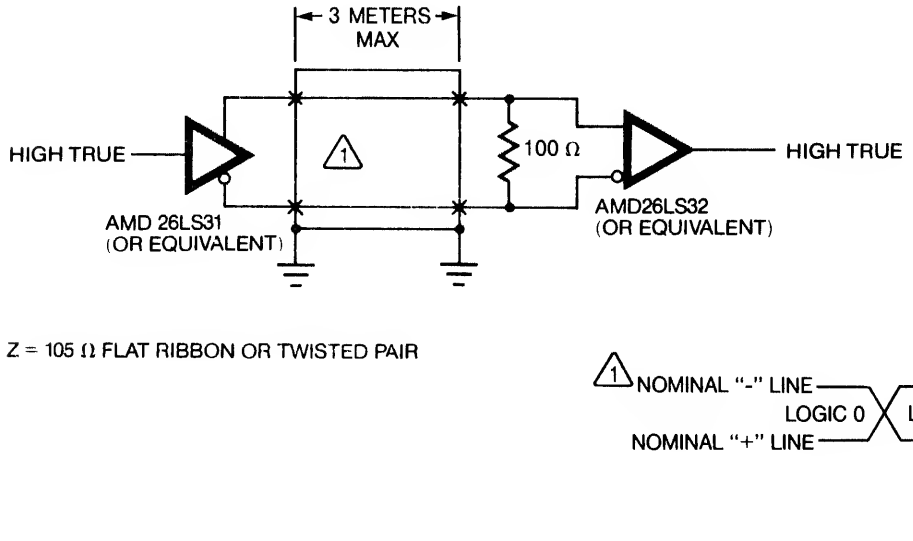
FALSE/DEACTIVE: 2.5 VDC to 5.25 VDC @ I= +250 uA (Open Collector)



CONTROL SIGNALS
DRIVER/RECEIVER COMBINATION
FIGURE 2

3.2 Data Line Drivers and Receivers

The data drivers and receivers are differential in nature. The recommended circuit is shown in Figure 3.



DATA LINE DRIVER/RECEIVER COMBINATION
FIGURE 3

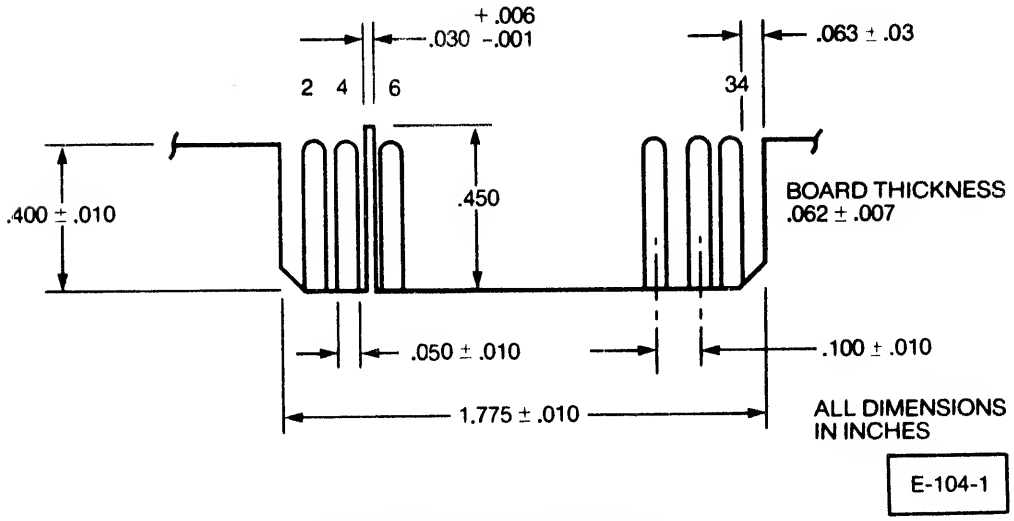
4.0 PHYSICAL INTERFACE

The electrical interface between the drive and the host controller is via four connectors:

1. J1 - Control signals (multiplexed)
2. J2 - Read/write signals (radial)
3. J3 - DC power input
4. J4 - Frame ground

4.1 J1/P1 Connector

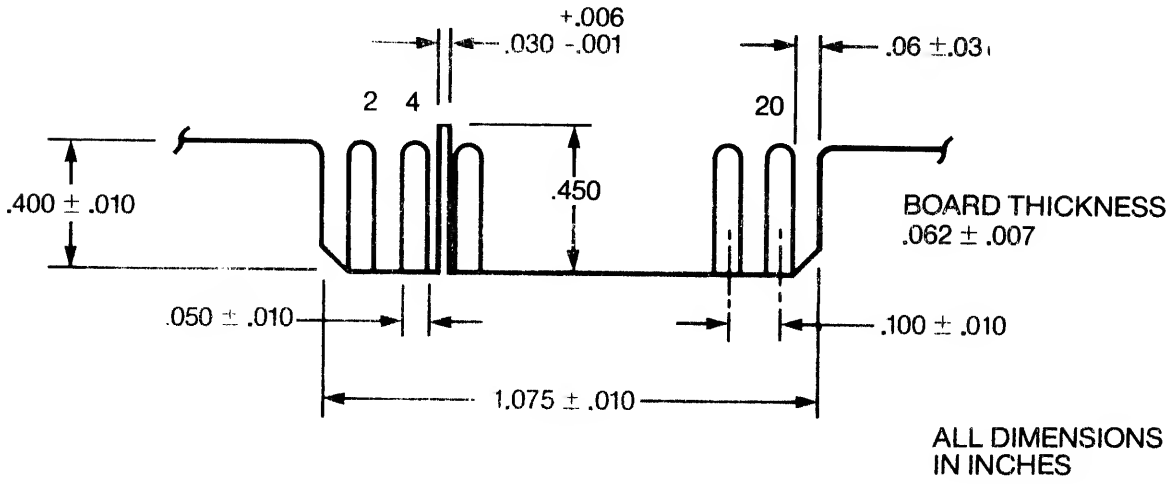
Connection to J1 is via a 34 pin PCB edge connector. The dimensions for this connector are shown in Figure 4. The pins are numbered 1 through 34 with the even pins located on one side of the PCB. A key slot is provided between pins 4 and 6. The recommended mating connector for P1 is AMP ribbon connector P/N 88373-3 or equivalent. See Figure 7 for connector orientation.



J1 CONNECTOR DIMENSIONS
FIGURE 4

4.2 J2/P2 Connector

Connection of J2 is via a 20 pin PCB edge connector. The dimensions for the connector are shown in Figure 5 . The pins are numbered 1 through 20 with the even pins located on one side of the PCB. The recommended mating connector for P2 is AMP ribbon connector P/N 88373-6 or equivalent. A key slot is provided between pins 4 and 6. See Figure 7 for orientation.



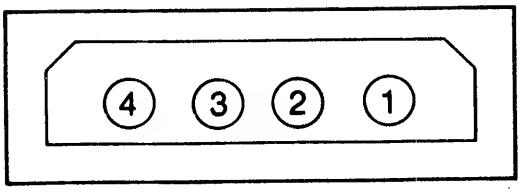
J2 CONNECTOR DIMENSIONS
FIGURE 5

4.3 J3/P3 Connector

The DC power connector (J3), is a 4 pin AMP MATE-N-LOCK connector P/N 350543-1. An alternate connector is AMP MATE-N-LOCK P/N 641737-1 (right angle). The recommended mating connector (P3) is AMP P/N 1-480424-0 utilizing AMP pins P/N 350078-4 (strip) or P/N 61173-4 (loose piece). Equivalents of these part numbers are permissible. J3 pins are numbered as shown in Figure 6. Pin assignments are shown in Table 1. See Figure 7 for connector orientation.

4.4 J4/P4 Frame Ground Connector

The frame ground connection is a Faston type connection, AMP P/N 61761-2 or equivalent. The recommended mating connection is AMP 62187-1 or equivalent. If wire is used, the hole in J4 will accomodate a wire size of 18AWG maximum.



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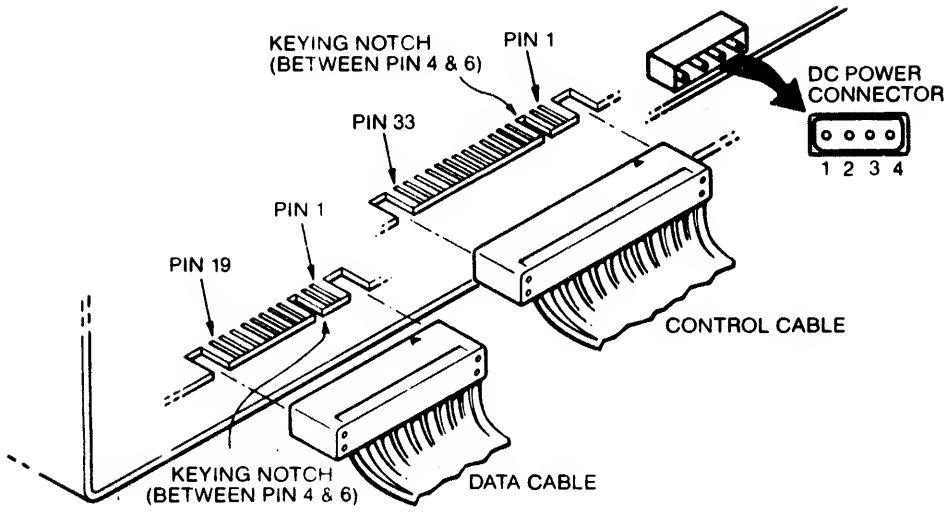
J3 CONNECTOR
FIGURE 6

J3 CONNECTOR PIN	VOLTAGE
1	+12V DC ±5%
2	12V RETURN
3	5V RETURN
4	+ 5V DC ±5%

E-106-0

J3 CONNECTOR PIN ASSIGNMENTS
TABLE 1



(BACK-END VIEW OF DRIVE)

E-107-0

TYPICAL PCB CONNECTOR ORIENTATION
FIGURE 7

5.0 DISK DRIVE IMPLEMENTATION -- SERIAL MODE

This section describes the interface lines, hardware, and interface protocols necessary to implement the SERIAL mode disk drive version of the ESDI. Pin assignments for connectors J1 and J2 are shown in Figures 9 and 10 along with Tables 3 and 4.

5.1 Control Input Lines

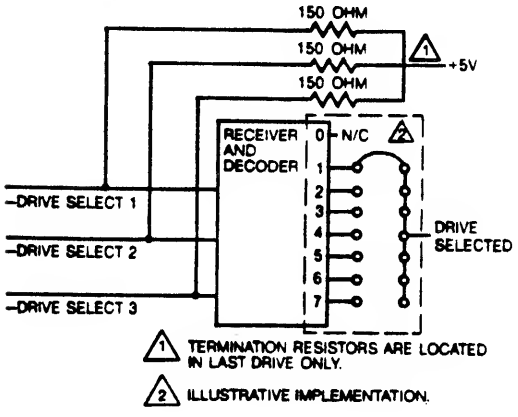
The control input signals are of two types: those to be multiplexed in a multiple drive system and those intended to do the multiplexing. The control input signals to be multiplexed are WRITE GATE, READ GATE, HEAD SELECT 2^0, HEAD SELECT 2^1, HEAD SELECT 2^2, HEAD SELECT 2^3, TRANSFER REQ and COMMAND DATA. The signals to do the multiplexing are DRIVE SELECT 1, DRIVE SELECT 2, and DRIVE SELECT 3.

ADDRESS MARK ENABLE is a control input in the radial cable. It is not multiplexed.

NOTE: Any lines not used should be terminated.

5.1.1 Drive Select

The three DRIVE SELECT lines are to be decoded for drive select. Decode 000 shall be a no select. See Figure 8 and Table 2.



E-108-0

DRIVE SELECT TERMINATION
FIGURE 8

DRIVE SELECTED	DRIVE SELECT 3	DRIVE SELECT 2	DRIVE SELECT 1
NONE	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

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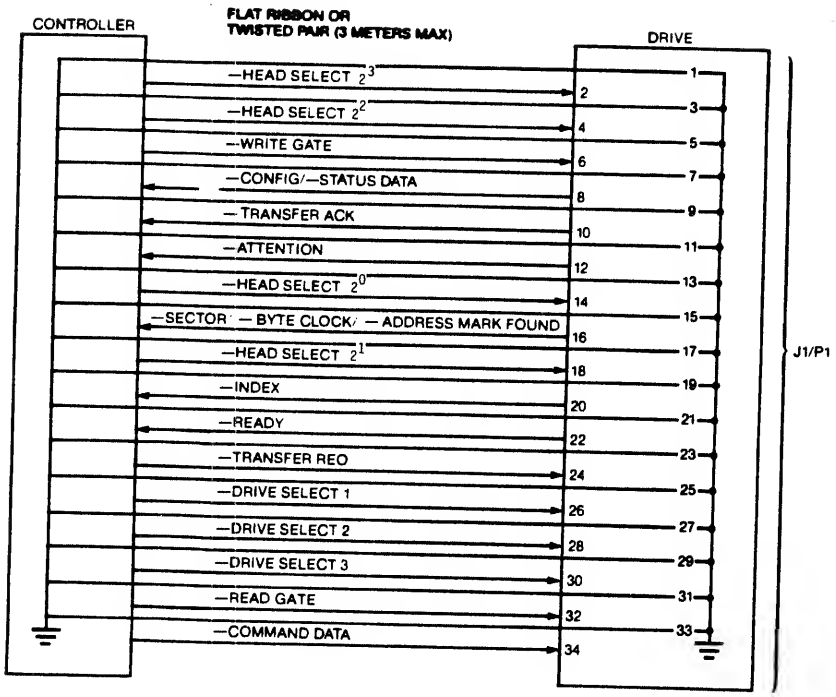
DRIVE SELECTION MATRIX
TABLE 2



E-110-1

CONTROL CABLE (J1/P1) SIGNALS
(DISK IMPLEMENTATION - SERIAL MODE)
FIGURE 9

SIGNAL NAME	SIGNAL PIN	GROUND PIN
—HEAD SELECT 2^3	2	1
—HEAD SELECT 2^2	4	3
—WRITE GATE	6	5
—CONFIG/—STATUS DATA	8	7
—TRANSFER ACK	10	9
—ATTENTION	12	11
—HEAD SELECT 2^0	14	13
—SECTOR/—BYTE CLOCK/—ADDRESS MARK FOUND	16	15
—HEAD SELECT 2^1	18	17
—INDEX	20	19
—READY	22	21
—TRANSFER REQ	24	23
—DRIVE SELECT 1	26	25
—DRIVE SELECT 2	28	27
—DRIVE SELECT 3	30	29
—READ GATE	32	31
—COMMAND DATA	34	33

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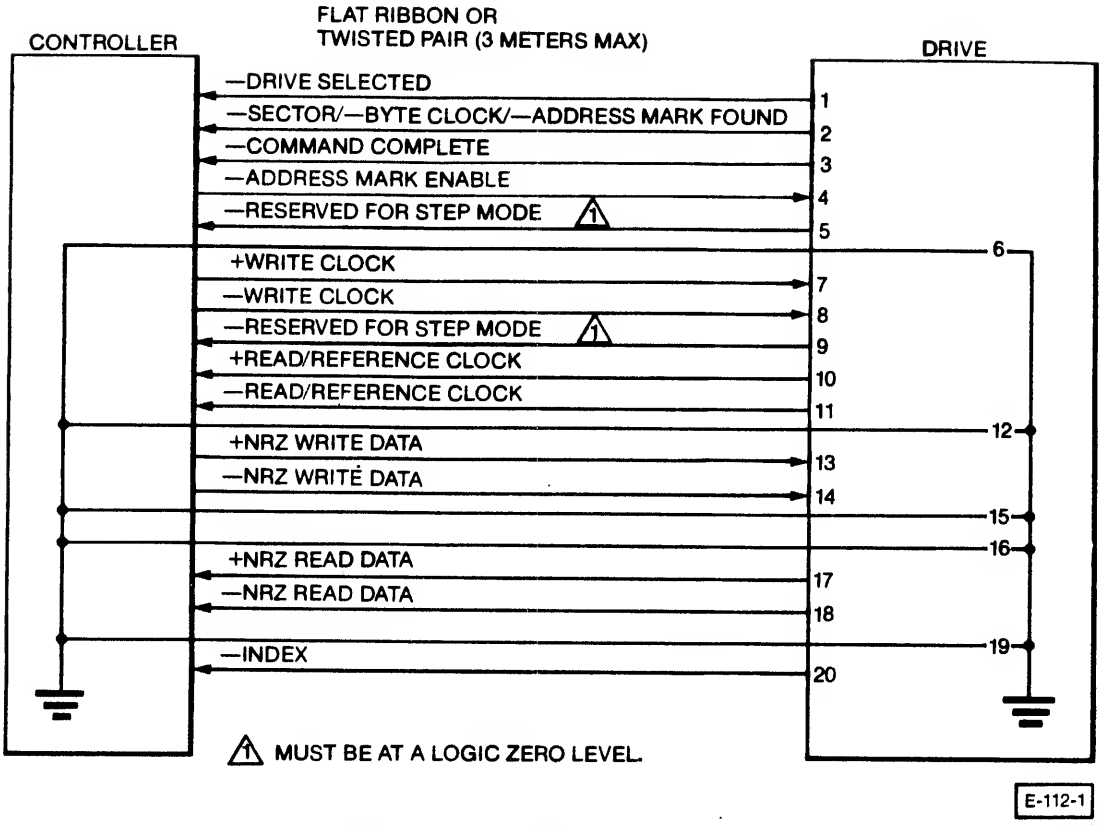
CONTROL CABLE (J1/P1) PIN ASSIGNMENTS
(DISK IMPLEMENTATION - SERIAL MODE)
TABLE 3



DATA CABLE (J2/P2) SIGNALS
(DISK IMPLEMENTATION - SERIAL MODE)
FIGURE 10

SIGNAL NAME	SIGNAL PIN	GROUND PIN
—DRIVE SELECTED	1	
-SECTOR-BYTE CLOCK-ADDRESS MARK FOUND	2	
—SEEK COMPLETE	3	
—ADDRESS MARK ENABLE	4	
—RESERVED FOR STEP MODE	5	6
+/—WRITE CLOCK	7/8	
RESERVED FOR STEP MODE	9	
+/—READ REF CLOCK	10/11	12
+/—NRZ WRITE DATA	13/14	15/16
+/—NRZ READ DATA	17/18	19
—INDEX	20	

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DATA CABLE (J2/P2) PIN ASSIGNMENTS
(DISK IMPLEMENTATION - SERIAL MODE)
TABLE 4

5.1.2 Head Select 2^0, 2^1, 2^2, and 2^3

These four lines allow selection of each individual read/ write head in a binary coded sequence. HEAD SELECT 2^0 is the least significant line. Heads are numbered 0 through 15. When all HEAD SELECT lines are high (inactive), head 0 will be selected. Addressing more than 16 heads is allowed by use of the SELECT HEAD GROUP command.

Head addressing is continuous from 0 through both removeable and fixed drives. If removeable drive is present, head 0 will be on the removeable media drive.

Addressing more heads than contained in the drive will result in a write fault when attempting to perform a write operation.

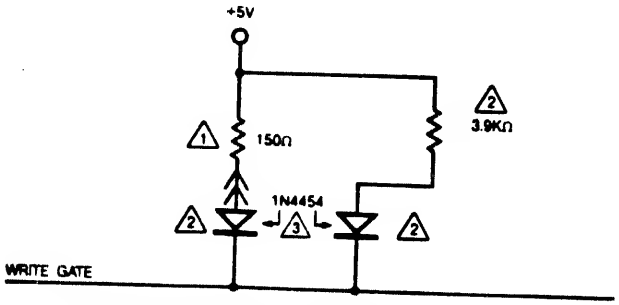
A 150 OHM resistor pack allows for line termination.

5.1.3 Write Gate

The active state of this signal, or low level, enables write data to be written on the disk.

The high to low transition of this signal creates a write splice and initiates the writing of the data PLO Sync field by the drive. See Figures 23 and 25. When formatting, WRITE GATE should be deactivated for 2 bit times minimum between the address area and the data area to identify to the drive the beginning of the data PLO sync field.

This line shall be protected from terminator power loss by implementation of the circuit shown in Figure 11.



1 PART OF THE TERMINATOR RESISTOR PACK IN THE LAST DRIVE OF THE DAISY CHAIN.

2 PERMANENTLY LOCATED IN THE DRIVE.

3 OR EQUIVALENT PART.

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WRITE GATE TERMINATION
FIGURE 11

5.1.4 Read Gate

The active state of this signal, or low level, enables data to be read from the disk. This signal should become active only during a PLO sync field and at least the number of bytes defined by the drive prior to the ID or Data Sync Bytes. The PLO sync field length is determined by the response to the REQUEST PLO SYNC FIELD LENGTH command. Read gate must be false when passing over a write splice area.

A 150 OHM resistor pack allows for line termination.

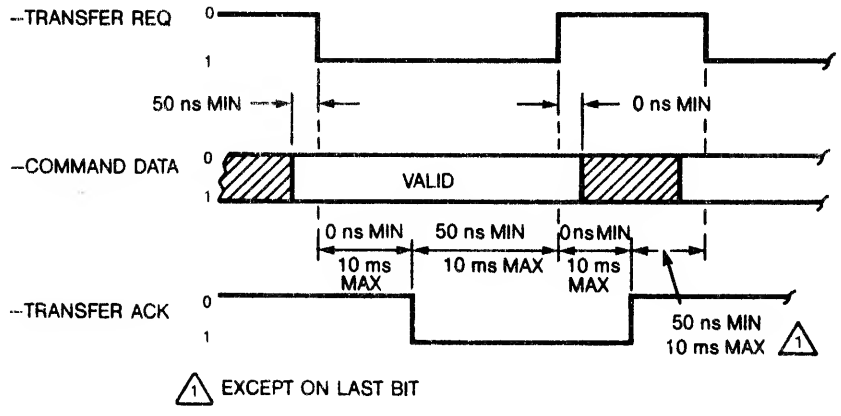
5.1.5 Command Data

When presenting a command, 16 information bits of serial data, plus parity, will be presented on this line. This data is to be controlled by the handshake protocol with signals TRANSFER REQ and TRANSFER ACK. Upon receipt of this serial data, the drive will perform the required function as specified by the bit configuration. Data is transmitted MSB first. See Table 5 for the meaning of the various bit combinations. See Figure 12A for timing.

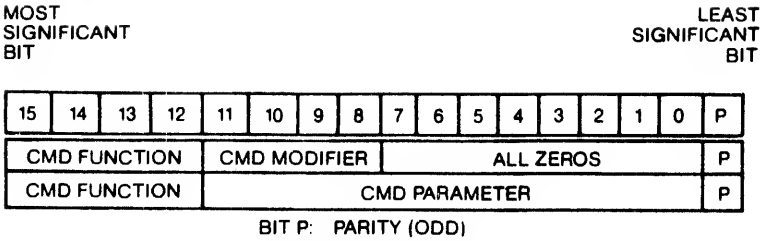
The parity utilized in all commands shall be odd. The parity bit shall be a "1" when the number of "1's" in a 16 bit command is an even number. The number of "1" bits in the command, plus parity, shall be an odd number.

No communications should be attempted unless the COMMAND COMPLETE line is true. Note: This line must be at a logic 0 when not in use.

A 150 OHM resistor pack allows for line termination.



ONE BIT TRANSFER TIMING — TO DRIVE
FIGURE 12A



BIT P: PARITY (ODD)

COMMAND DATA WORD STRUCTURE
FIGURE 12B

E-116-0

CMD FUNCTION BIT 15 14 13 12	CMD FUNCTION DEFINITION	CMD MODIFIER APPLICABLE (BITS 11–8)	CMD PARAMETER APPLICABLE (BITS 11–0)	STATUS/CONFIGURATION DATA RETURNED TO CONTROLLER
0 0 0 0	SEEK	NO	YES	NO
0 0 0 1	RECALIBRATE	NO	NO	NO
0 0 1 0	REQUEST STATUS	YES	NO	YES
0 0 1 1	REQUEST CONFIGURATION	YES	NO	YES
0 1 0 0	SELECT HEAD GROUP (OPTIONAL)	NO	YES	NO
0 1 0 1	CONTROL	YES	NO	NO
0 1 1 0	DATA STROBE OFFSET	YES	NO	NO
0 1 1 1	TRACK OFFSET	YES	NO	NO
1 0 0 0	INITIATE DIAGNOSTICS (OPTIONAL)	NO	NO	NO
1 0 0 1	SET BYTES PER SECTOR (OPTIONAL)	NO	YES	NO
1 0 1 0	RESERVED	—	—	—
1 0 1 1	RESERVED	—	—	—
1 1 0 0	RESERVED	—	—	—
1 1 0 1	RESERVED	—	—	—
1 1 1 0	RESERVED	—	—	—
1 1 1 1	RESERVED	—	—	—

NOTES: 1. ALL UNUSED OR NOT APPLICABLE LOWER ORDER BITS MUST BE ZERO.
2. ANY "RESERVED" OR COMMAND FUNCTION RECEIVED SHALL BE TREATED AS AN INVALID COMMAND.
3. SIMULTANEOUS DATA STROBE AND TRACK OFFSETS ARE ALLOWED BY MULTIPLE COMMANDS.

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COMMAND (CMD) DATA DEFINITION
TABLE 5

5.1.5.1 Command Data bits 15 thru 12 decode definition

SEEK (0000): This command causes the drive to seek to the cylinder indicated in Bits 0 thru 11. A SEEK command will restore data strobe and track offsets to zero.

RECALIBRATE (0001): This command causes the actuator to return to cylinder 0000. A RECALIBRATE command will restore data strobe and track offsets to zero.

REQUEST STATUS (0010): This command causes the drive to send 16 bits (see Table 12, page 21) of standard or vendor unique status information to the controller as determined by the command modifier bits. The parity utilized in all status responses shall be odd.

Request Standard Status: When the command modifier bits (11-8) of the REQUEST STATUS command is 0000, the drive will respond with 16 bits of standard status. Bits 15-12 of this status are defined as state bits which do not cause ATTENTION to be asserted. Bits 11-0 of this status are fault or change of status bits that cause ATTENTION to be asserted each time one is set. See section 5.2.3.2 for response protocol and format of the status response from the drive.

Request Vendor Unique Status: When the command modifier bits (11-8) of the REQUEST STATUS command is 0001 through 1111, the drive responds with vendor unique status (undefined in this specification). The number of words available is specified by configuration data. Each word of vendor unique status is requested using a different command modifier configuration. This command modifier for the first word is 0001 and subsequent words are requested by incrementing the command modifier.

REQUEST CONFIGURATION (0011): This command causes the drive to send 16 bits (Table 10 and 11, page 20) of configuration data to the controller. The parity utilized in all configuration responses shall be odd. The specific configuration requested is specified by bits 11-8 of the command as shown below in Table 6:

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	GENERAL CONFIGURATION OF DRIVE AND FORMAT
0	0	0	1	NUMBER OF CYLINDERS, FIXED
0	0	1	0	NUMBER OF CYLINDERS, REMOVABLE
0	0	1	1	NUMBER OF HEADS
0	1	0	0	MINIMUM UNFORMATTED BYTES PER TRACK
0	1	0	1	UNFORMATTED BYTES PER SECTOR (HARD SECTOR ONLY)
0	1	1	0	SECTORS PER TRACK (HARD SECTOR ONLY)
0	1	1	1	MINIMUM BYTES IN ISG FIELD*
1	0	0	0	MINIMUM BYTES PER PLO SYNC FIELD
1	0	0	1	NUMBER OF WORDS OF VENDOR UNIQUE STATUS AVAILABLE

*NOT INCLUDING INTERSECTOR SPEED TOLERANCE

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REQUEST CONFIGURATION MODIFIER BITS
TABLE 6

SELECT HEAD GROUP (0100): This optional command causes the drive to select a group of 16 heads. Heads 0-15 are considered as group 0. Bits 7-4 are used to indicate the group to be selected. Bit 4, if a one, causes head group 1 (heads 16-31) to be selected. Bit 5 will cause head group 2 to be selected. The individual head selected within each group is controlled by the four head select lines.

CONTROL (0101): This command causes the control operations specified by bits 11-8 to be performed as shown below in Table 7:

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	RESET INTERFACE ATTENTION AND STANDARD STATUS (BITS 0- 11)
0	0	0	1	RESERVED
0	0	1	0	STOP SPINDLE MOTOR (OPTIONAL)
0	0	1	1	START SPINDLE MOTOR (OPTIONAL)
0	1	0	0	RESERVED
0	1	0	1	RESERVED
0	1	1	0	RESERVED
0	1	1	1	RESERVED
1	X	X	X	RESERVED

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CONTROL COMMAND MODIFIER BITS
TABLE 7

DATA STROBE OFFSET (0110): This optional command causes the drive to offset the data strobe in the direction and amount specified by Bits 11-8 as shown below in Table 8:

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	RESTORE OFFSET TO 0
0	0	0	1	RESTORE OFFSET TO 0
0	0	1	0	EARLY OFFSET 1
0	0	1	1	LATE OFFSET 1
0	1	0	0	EARLY OFFSET 2
0	1	0	1	LATE OFFSET 2
0	1	1	0	EARLY OFFSET 3
0	1	1	1	LATE OFFSET 3
1	X	X	X	RESERVED

DATA STROBE COMMAND MODIFIER BITS
TABLE 8

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Seek or recalibrate commands restore offsets to zero. Simultaneous Data Strobe and Track offsets are allowed by use of multiple commands.

TRACK OFFSET (0111): This optional command causes the drive to perform a track offset in the direction and amount specified by Bits 11-8 as shown below in Table 9:

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	RESTORE OFFSET TO 0
0	0	0	1	RESTORE OFFSET TO 0
0	0	1	0	POSITIVE OFFSET 1
0	0	1	1	NEGATIVE OFFSET 1
0	1	0	0	POSITIVE OFFSET 2
0	1	0	1	NEGATIVE OFFSET 2
0	1	1	0	POSITIVE OFFSET 3
0	1	1	1	NEGATIVE OFFSET 3
1	X	X	X	RESERVED

TRACK OFFSET COMMAND MODIFIER BITS
TABLE 9

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Seek and recalibrate commands restore offsets to zero. Simultaneous Track and Data Strobe offsets are allowed by use of multiple commands.

Drives that implement only one value of offset, Data Strobe or Track, shall respond to unimplemented offset commands as a legal offset function.

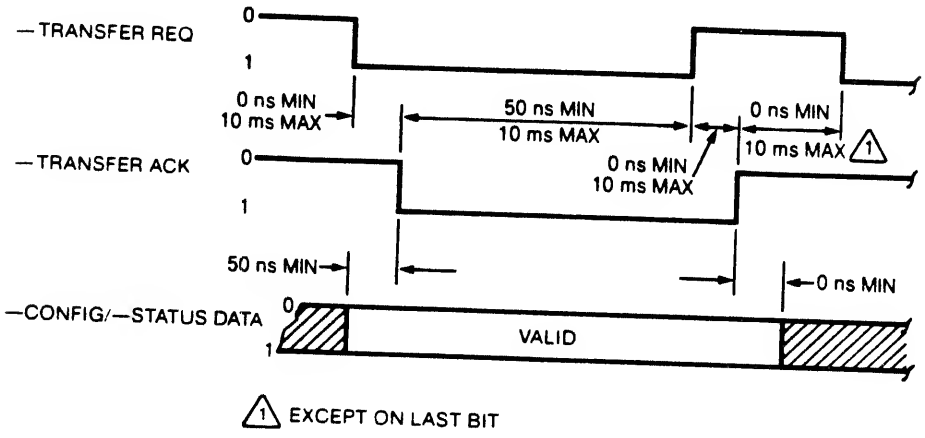
INITIATE DIAGNOSTICS (1000): This optional command causes the drive to perform internal diagnostics. COMMAND COMPLETE indicates the completion of the diagnostics. ATTENTION with COMMAND COMPLETE indicates that a fault was encountered and status should be requested to determine the proper course of action.

SET UNFORMATTED BYTES PER SECTOR (1001): This optional command causes the drive to set the number of unformatted bytes per sector indicated in bits 11-0 (if implemented). This command is valid only if the drive is configured to be in the drive hard sectored mode. This command is used only if the drive uses a settable counter for the number of bytes per sector and that counter is controllable from the interface.

CODES 1010 THRU 1111: Codes reserved for future definition.

5.1.6 Transfer Request (Transfer Req)

This line functions as a handshake signal in conjunction with TRANSFER ACK during command and configuration/status transfers. See Figures 12A, page 12, and Figure 13, page 17 for timing.



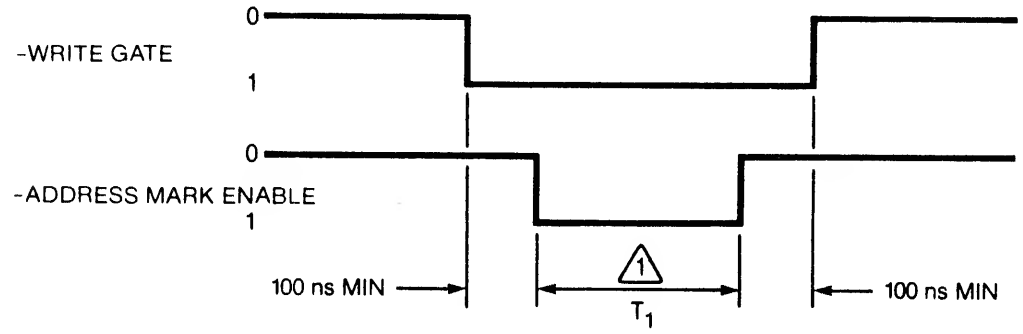
ONE BIT TRANSFER TIMING — FROM DRIVE
FIGURE 13

5.1.7 Address Mark Enable

This signal, when active with Write Gate, causes an Address Mark to be written. ADDRESS MARK ENABLE shall be active for 24 bit times. See Figure 14 for timing. The address mark written shall be left to the drive manufacturer's discretion.

ADDRESS MARK ENABLE, when active without WRITE GATE or READ GATE, causes a search for Address Marks. If WRITE GATE is true, the low to high transition, or deassertion, of this signal causes the drive to begin writing the ID PLO Sync field. See Figures 23, page 37, and Figure 25, page 40.

This line must be permanently terminated in the drive. See figure 2.



WRITE ADDRESS MARK TIMING
FIGURE 14

In fixed sector drives, ADDRESS MARK ENABLE does not cause an Address Mark to be written on the media. The trailing edge of ADDRESS MARK ENABLE with WRITE GATE true initiates the writing of the header PLO sync field.

5.2 Control Output Lines

The output control signals are driven with an open collector output stage capable of sinking a maximum of 48mA at low level or true state with maximum voltage of 0.4V measured at the driver. When the line driver is in the high level or false state, the driver transistor is off and collector leakage current is a maximum of 250uA.

All J1 output lines are enabled by their respective DRIVE SELECT decodes.

Figure 2 shows the recommended circuit.

5.2.1 Drive Selected

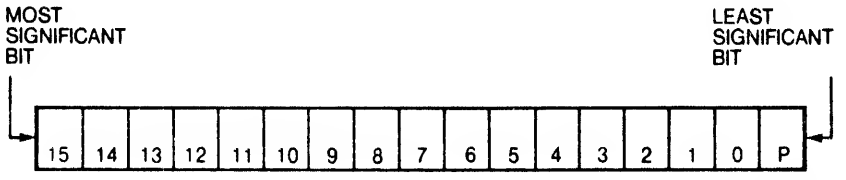
A status line provided at the J2/P2 connector to inform the host system of the selection status of the drive. The DRIVE SELECTED line is driven by a TTL open collector driver as shown in Figure 2. This signal will go active only when the drive is selected as defined in section 5.1.1. (page 8). The DRIVE SELECT lines at J1/P1 are activated by the host system.

5.2.2 Ready

This signal indicates that the spindle is up to speed. This interface signal when true, together with COMMAND COMPLETE indicates that the drive is ready to read, write or, seek. When the line is false, all writing and seeking is inhibited.

5.2.3 Configuration/Status Data (Config/Status)

The drive presents serial data on this line upon request from the controller. See Figure 16 for typical operation. This config-status serial data will be presented to the interface and transferred using the handshake protocol with signals TRANSFER REQ and TRANSFER ACK. See Figure 13. Once initiated, 16 bits plus parity will be transmitted MSB first. The parity utilized shall be odd.



CONFIGURATION/STATUS DATA WORD STRUCTURE
FIGURE 15

5.2.3.1 Configuration Response Bits

In response to the REQUEST CONFIGURATION command (see section 5.1.5.1 page 14) 16 bits of configuration information is returned to the controller.

If the command modifier bits (11-8) were 0000, the general configuration status information shown below is returned.

BIT POSITION	FUNCTION
15	TAPE DRIVE
14	FORMAT SPEED TOLERANCE GAP REQUIRED
13	TRACK OFFSET OPTION AVAILABLE
12	DATA STROBE OFFSET OPTION AVAILABLE
11	ROTATIONAL SPEED TOLERANCE IS >0.5%
10	TRANSFER RATE >10MHz
9	TRANSFER RATE >5MHz ≤10MHz
8	TRANSFER RATE ≤5MHz
7	REMOVABLE CARTRIDGE DRIVE
6	FIXED DRIVE
5	SPINDLE MOTOR CONTROL OPTION IMPLEMENTED
4	HEAD SWITCH TIME >15μs*
3	RLL ENCODED (NOT MFM)
2	CONTROLLER SOFT SECTORED (ADR MARK)
1	DRIVE HARD SECTORED (SECTOR PULSES)
0	CONTROLLER HARD SECTORED (BYTE CLOCK)

*COMMAND COMPLETE MUST BE DEACTIVATED WITHIN 15μsec OF A HEAD CHANGE

GENERAL CONFIGURATION RESPONSE BITS
TABLE 10

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If other command modifier bits were used, the specific configuration information shown below is returned for each CONFIGURATION command with those modifiers.

COMMAND MODIFIER BITS				CONFIGURATION RESPONSE
11	10	9	8	
0	0	0	1	NUMBER OF CYLINDERS, FIXED
0	0	1	0	NUMBER OF CYLINDERS, REMOVABLE (ZERO IF NOT REMOVABLE MEDIA DRIVE)
0	0	1	1	NUMBER OF HEADS BITS 15-8: REMOVABLE DRIVE HEADS BITS 7-0: FIXED HEADS
0	1	0	0	MINIMUM UNFORMATTED BYTES PER TRACK
0	1	0	1	UNFORMATTED BYTES PER SECTOR (HARD SECTOR ONLY)
0	1	1	0	SECTORS PER TRACK (DRIVE HARD SECTOR ONLY) BITS 15-8: SPARE BITS 7-0: SECTORS PER TRACK
0	1	1	1	MINIMUM BYTES IN ISG FIELD (NOT INCLUDING INTERSECTOR SPEED TOLERANCE) BITS 15-8: ISG BYTES AFTER INDEX BITS 7-0: BYTES PER ISG
1	0	0	0	MINIMUM BYTES PER PLO SYNC FIELD BITS 15-8: SPARE BITS 7-0: BYTES PER PLO SYNC FIELD
1	0	0	1	NUMBER OF WORDS OF VENDOR UNIQUE STATUS AVAILABLE BITS 15-4: SPARE BITS 3-0: NUMBER OF VENDOR UNIQUE STATUS WORDS

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SPECIFIC CONFIGURATION RESPONSE BITS
TABLE 11

5.2.3.2 Status Response Bits

In response to the REQUEST STATUS command (See section 5.1.5.1, page 14) 16 bits of status information is returned to the controller.

Bits 15-12 of the status are defined as state bits which do not cause ATTENTION to be asserted. Bits 11-0 are fault or change of status bits that cause ATTENTION to be asserted.

BIT POSITION	FUNCTION
15	RESERVED
14	REMOVABLE MEDIA NOT PRESENT
13	WRITE PROTECTED, REMOVABLE MEDIA
12	WRITE PROTECTED, FIXED MEDIA
11	RESERVED
10	RESERVED
9	SPINDLE MOTOR STOPPED*
8	POWER ON RESET CONDITIONS EXIST (RECONFIGURATION OR START SPINDLE MOTOR COMMAND MAY BE REQUIRED
7	COMMAND DATA PARITY FAULT
6	INTERFACE FAULT
5	INVALID OR UNIMPLEMENTED COMMAND FAULT
4	SEEK FAULT
3	WRITE GATE WITH TRACK OFFSET FAULT
2	VENDOR UNIQUE STATUS AVAILABLE
1	WRITE FAULT**
0	REMOVABLE MEDIA CHANGED (REMOVABLE MEDIA HAS BEEN CHANGED SINCE LAST STATUS REQ)

*SPINDLE MOTOR IS STOPPED DUE TO PREVIOUS COMMAND TO STOP OR THE DRIVE IS IN POWER ON RESET CONDITION.

** CONDITIONS THAT CAN CAUSE WRITE FAULT ARE:

a. Write current in a head without WRITE GATE active or no write current with WRITE GATE active and the drive selected.

b. Multiple heads selected, no head selected, or improperly selected with WRITE GATE active.

c. WRITE GATE active to a write protected drive.

d. Simultaneous activation of READ GATE and WRITE GATE.

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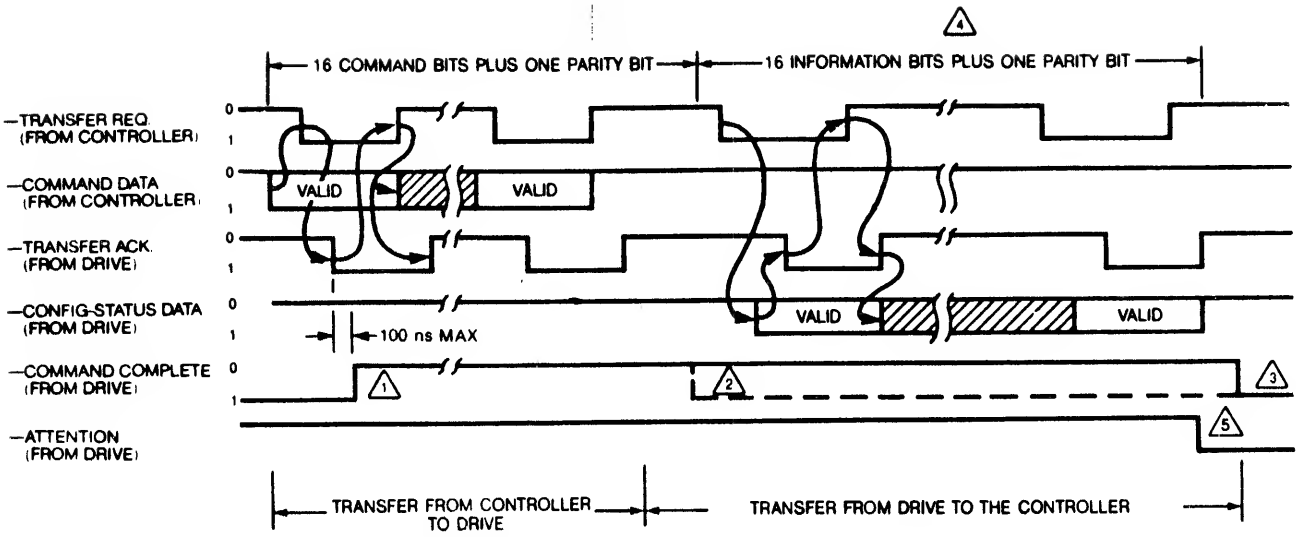
STANDARD STATUS RESPONSE BITS
TABLE 12



1. COMMAND COMPLETE IS DEACTIVATED FOR ALL COMMANDS TO THE DRIVE.
2. COMMAND COMPLETE IS ACTIVATED TO SIGNIFY COMPLETION OF EXECUTION OF A COMMAND. APPLICABLE FOR ALL COMMANDS.
3. COMMAND COMPLETE IS ACTIVATED TO SIGNIFY COMPLETION OF THE REQUESTED CONFIGURATION/STATUS TRANSFER.
4. APPLICABLE FOR ALL REQUEST STATUS AND CONFIGURATION COMMANDS.
5. IF AN ERROR WAS ENCOUNTERED DURING THE CURRENT COMMAND, ATTENTION MUST BE ACTIVATED AT LEAST 100 ns BEFORE COMMAND COMPLETE IS ACTIVATED.

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TYPICAL SERIAL OPERATION(S)
FIGURE 16

5.2.4 Transfer Acknowledge (Transfer Ack)

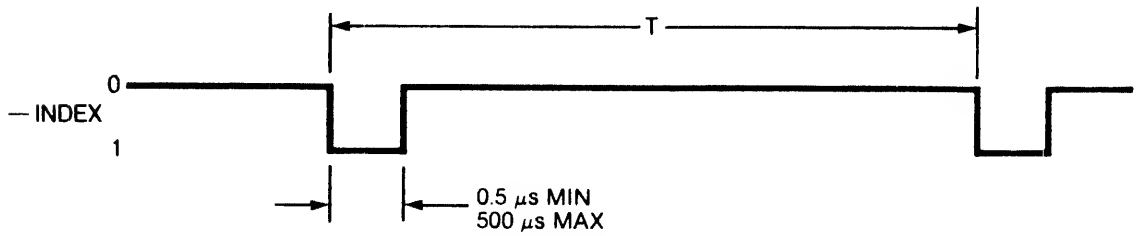
This signal functions as a handshake signal along with TRANSFER REQ during COMMAND and CONFIGURATION-STATUS transfers. See Figures 12A and 13.

5.2.5 Attention

This output is asserted when the drive wants the controller to request its standard status. Generally, this is a result of a fault condition or a change of status. Writing is inhibited when ATTENTION is asserted. ATTENTION is deactivated by the Reset Interface Attention command (section 5.1.5.1).

5.2.6 Index

This pulse is provided by the drive once each revolution to indicate the beginning of a track. Normally, this signal is high and makes the transition to low to indicate INDEX. Only the transition at the leading edge of the pulse is accurately controlled. The period (T) of this signal is the reciprocal of the rotational speed, Figure 17. This signal is available on the command cable J1/P1 (gated) and on the data cable J2/P2 (ungated).



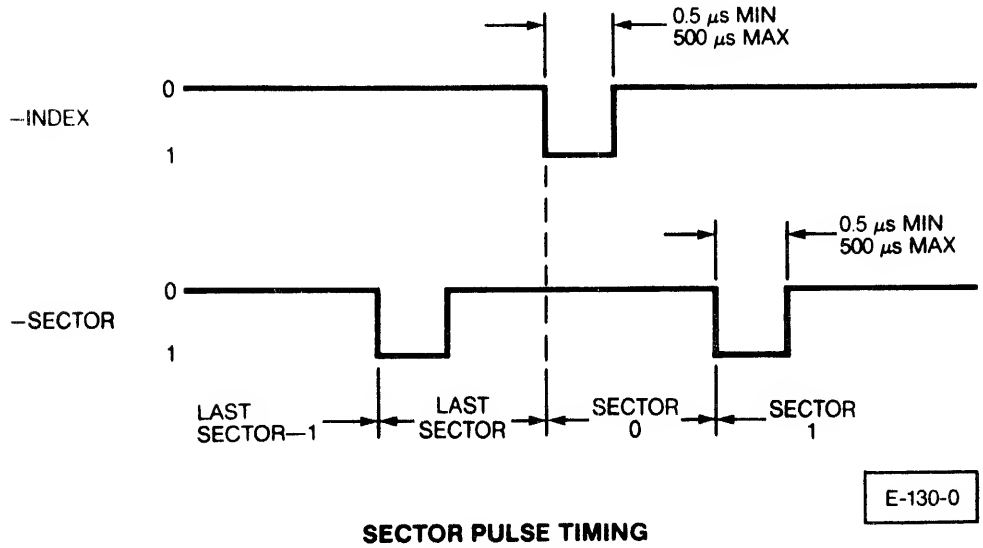
INDEX TIMING
FIGURE 17

5.2.7 Sector/Byte Clock/Address Mark Found

These three signals are mutually exclusive and therefore may share this line. The signal that is used is determined by the NRZ data transfer control implementation. These signals are available on the command cable J1/P1 (gated) and on the data cable J2/P2 (ungated). One of these three signals must be implemented by the drive manufacturer.

5.2.7.1 Sector (Drive Hard Sector)

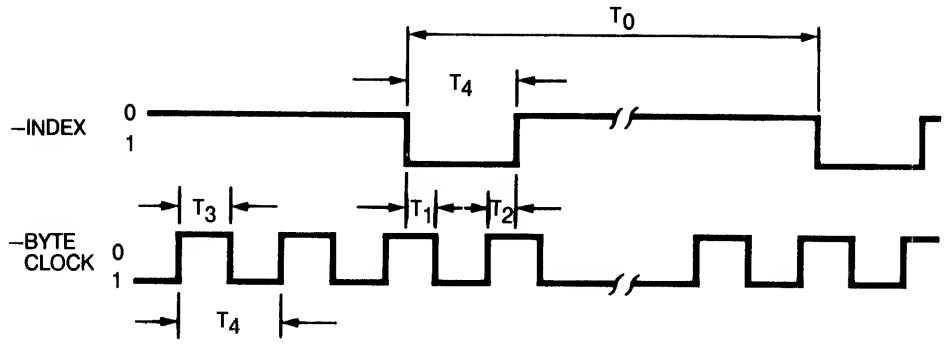
This optional interface signal indicates the start of a sector. No short sectors are allowed. The leading edge of the sector pulses is the only edge that is accurately controlled. The index pulse indicates sector zero. See Figure 18.



SECTOR PULSE TIMING
FIGURE 18

5.2.7.2 Byte Clock (Controller Hard Sector)

This signal occurs once per every eight Reference clock periods. This signal is provided for the controller to count the desired number of Byte Clocks to determine the sector size and beginning sector locations. The inter-relationship of INDEX and BYTE CLOCK is shown in Figure 19. This signal is continuously transmitted if the disk is up to speed and the heads are positioned over the recording zone of the disk. This clock does not have a fixed phase relationship to the recorded data.



T_0 = DISK ROTATIONAL PERIOD = INVERSE OF DISK REVOLUTIONS PER SECOND
T_1 = (0.16) x (T_4) TO (0.25) x (T_4)
T_2 = (0.25) x (T_4) TO (0.33) x (T_4)
T_3 = (0.40) x (T_4) TO (0.6) x (T_4)
T_4 = 8 TIMES THE REFERENCE CLOCK PERIOD (T)
NOTE: TIMING IS NOMINAL AND MAY VARY DUE TO SPEED VARIATIONS.

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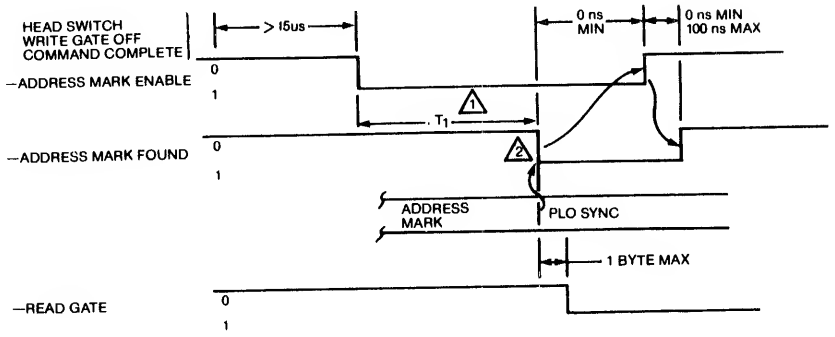
INDEX AND BYTE CLOCK RELATIONSHIP
FIGURE 19

5.2.7.3 Address Mark Found (Controller Soft Sector)

This signal indicates the detection of the end of an address mark. See Figure 20 for timing.



1 T_1 = 24 BIT TIMES MINIMUM.
2 LEADING EDGE INDICATES THE LOCATION OF THE END OF AN ADDRESS MARK.

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READ ADDRESS MARK TIMING
FIGURE 20

5.2.8 Command Complete

A status line provided at the J2/P2 connector. This is an ungated output from the drive which allows the host to monitor the drive's COMMAND COMPLETE status, during overlapped commands, without selecting the drive. This signal line will go false in the following cases:

1. A recalibration sequence is initiated (by drive logic) at power on, if the R/W heads are not over track zero.

2. Upon receipt of the first Command Data bit. COMMAND COMPLETE will stay false during the entire command sequence.

3. Within 15 usec from a head select change if head selection time is >15usec as indicated in CONFIGURATION DATA.

This signal is driven by an open collector driver as shown in Figure 2.

5.3 Data Transfer Lines

All lines associated with the transfer of data between the drive and the host system are differential in nature and may not be multiplexed. These lines are provided at the J2/P2 connectors on all drives.

Four pair of balanced signals are used for the transfer of data and clock :NRZ WRITE DATA , NRZ READ DATA, WRITE CLOCK, and READ/REFERENCE CLOCK. Figure 3 illustrates the recommended driver/receiver circuit.

5.3.1 NRZ Write Data

This is a differential pair that defines the data to be written on the track. This data will be clocked by the WRITE CLOCK signal. See Figure 21 for timing.

5.3.2 NRZ Read Data

The data recovered by reading previously written information is transmitted to the host system via the differential pair of NRZ READ DATA lines. This data is clocked by the READ CLOCK signal. See Figure 21 for timing. These lines must be held at a zero level until PLO sync has been obtained and data is valid.

5.3.3 Read/Reference Clock

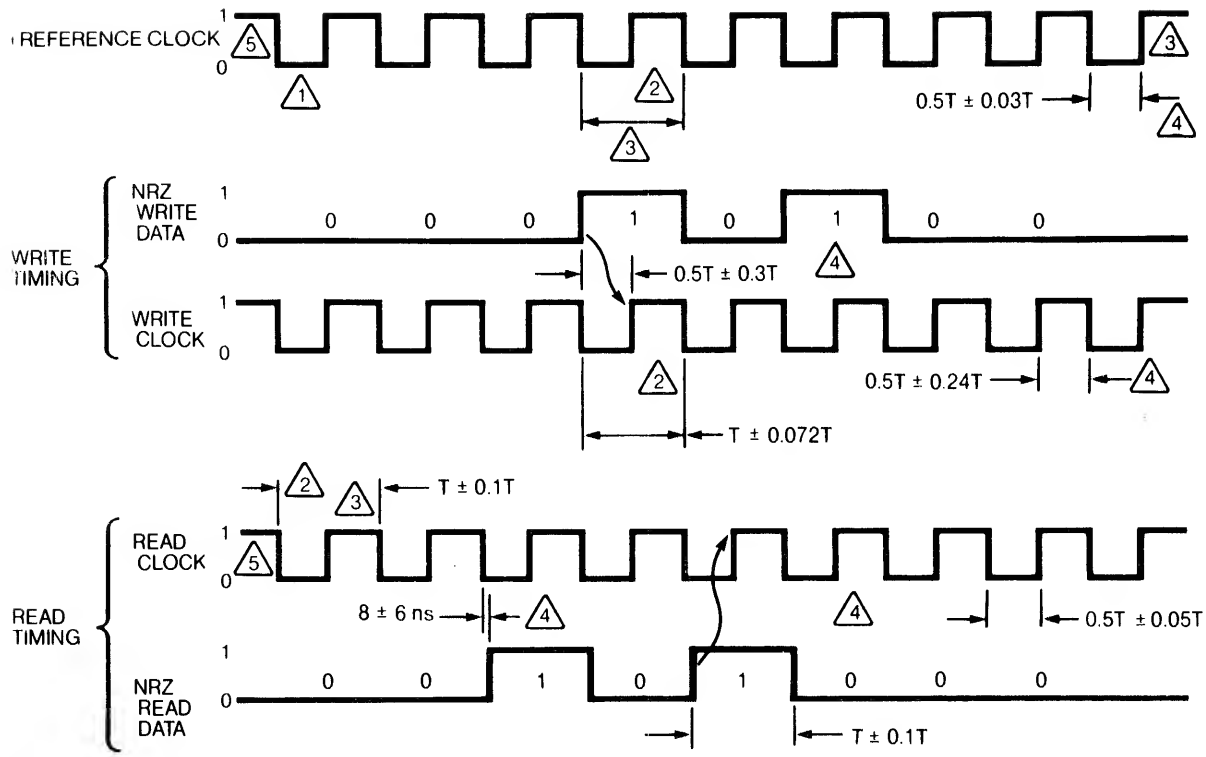
The timing diagram as shown in Figure 21 depicts the necessary sequence of events (with associated timing restrictions for proper read/write operation of the drive). The REFERENCE CLOCK signal from the drive will determine the data transfer rate. The transitions from REFERENCE CLOCK to READ CLOCK must be performed without glitches. Two missing clock cycles are permissible.

All controllers which meet the ESDI specification must be able to operate at a minimum of 10Mbits/second data transfer rate.

5.3.4 Write Clock

WRITE CLOCK is provided by the controller and must be at the bit data rate. This clock frequency shall be dictated by the READ/REFERENCE CLOCK during the write operation. See Figure 21 for timing.

WRITE CLOCK need not be continuously supplied to the drive. WRITE CLOCK should be supplied before beginning a write operation and should last for the duration of the write operation.



NOTES

1. ALL TIMES IN ns MEASURED AT I/O CONNECTOR OF THE DRIVE. T IS THE PERIOD OF THE CLOCK SIGNALS AND IS THE INVERSE OF THE REFERENCE OR READ CLOCK FREQUENCY.
2. SIMILAR PERIOD SYMMETRY SHALL BE IN ± 4ns BETWEEN ANY TWO ADJACENT CYCLES DURING READING OR WRITING.
3. EXCEPT DURING A HEAD CHANGE OR PLO SYNCHRONIZATION THE CLOCK VARIANCES FOR SPINDLE SPEED AND CIRCUIT TOLERANCES SHALL NOT VARY MORE THAN -5.5% to +5.0%. PHASE RELATIONSHIP BETWEEN REFERENCE CLOCK AND NRZ WRITE DATA OR WRITE CLOCK IS NOT DEFINED.
4. TIMING APPLICABLE DURING READING OR WRITING.
5. REFERENCE CLOCK IS VALID WHEN READ GATE IS INACTIVE. READ CLOCK IS VALID WHEN READ GATE IS ACTIVE AND PLO SYNCHRONIZATION HAS BEEN ESTABLISHED.
6. SEE FIGURE 3 FOR DEFINITION OF Ø AND 1 ON THESE DIFFERENTIAL SIGNAL LINES.

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NRZ READ/WRITE DATA TIMINGS
FIGURE 21

5.4 Read, Write, and Format Parameters

5.4.1 General Summary of Critical Read-Function Timing Parameters

Controller variations of the read timing are allowed if the following drive-dependent parameters are met:

a. Read Initialization Time.

A read operation may not be initiated until 15 us following a head change. Drives not able to meet 15 us must drop COMMAND COMPLETE upon a head switch.

b. Read-Gate Timing

Read Gate may not be enabled or true during a Write Splice area (Read Gate must be deactivated one bit time minimum before a Write Splice area and may be enabled one bit time minimum after a Write Splice area.)

c. Read Propagation Delay

Data (read) at the interface is delayed by up to 9 bit times from the data recorded on the disk media. See specific drive product specification for exact value.

d. Read Clock Timing

Read Clock and Read Data are valid within the number of PLO sync field bytes specified by the drive configuration after Read Enable and a PLO sync field is encountered The Interface Read/Reference Clock line may contain no transitions for up to two Reference Clock periods for transitions between reference and read clocks. The transition period will also be one-half of a Reference Clock period minimum with no shortened pulse widths.

5.4.2 General Summary of Critical Write-Function Parameters

Controller timing variations in the record-update function are allowed if the following drive-dependent write (and interrelated read) timing parameters are met:

a. Read-to-Write Recovery Time

Assuming head selection is stabilized, the time lapse from deactivating Read Gate to activiting Write Gate shall be five Reference Clock periods minimum.

b. Write Clock-to-Write Gate Timing

Write Clocks must precede Write Gate by a minimum of two and a half Reference Clock periods.

c. Write Driver Plus Data-Encoder Turn-On From Write Gate

The write driver plus data-encoder turn-on time (write splice width) is between 3 and 7 Reference Clock periods.

d. Write-Driver Turn-Off from Write Gate

To account for data-encoding delays, Write Gate must be held on for at least two byte times after the last bit of the information to be recorded.

e. Write-to-Read Recovery Time

The time lapse before READ GATE or ADDRESS MARK ENABLE can be activated after deactivating the Write Gate is 10us.

f. Head Switching Time

Write Gate must be deactivated at least 1 us before a head change.

Write Gate may not be activated until 15 us after a head change or COMMAND COMPLETE is true.

g. Reference Clocks Valid Time

The Read/Reference Clock lines will contain valid Reference Clocks within two Reference Clock periods after the deactivation of Read Gate. Pulse widths will not be shortened during the transition time but clock transitions may not occur for up to two Reference Clock periods.

h. Read Clocks Valid Time

The Read/Reference Clock line will contain valid Read clocks within two Clock periods after PLO synchronization is established. Pulse widths will not be shortened during the REFERENCE CLOCK to READ CLOCK transition time, but missing clocks may occur for up to two clock periods.

i. Write Propagation Delay

Write Data Received at the I/O connector will be delayed by the Write Data Encoder by up to 8 bit times maximum prior to being recorded on the media.

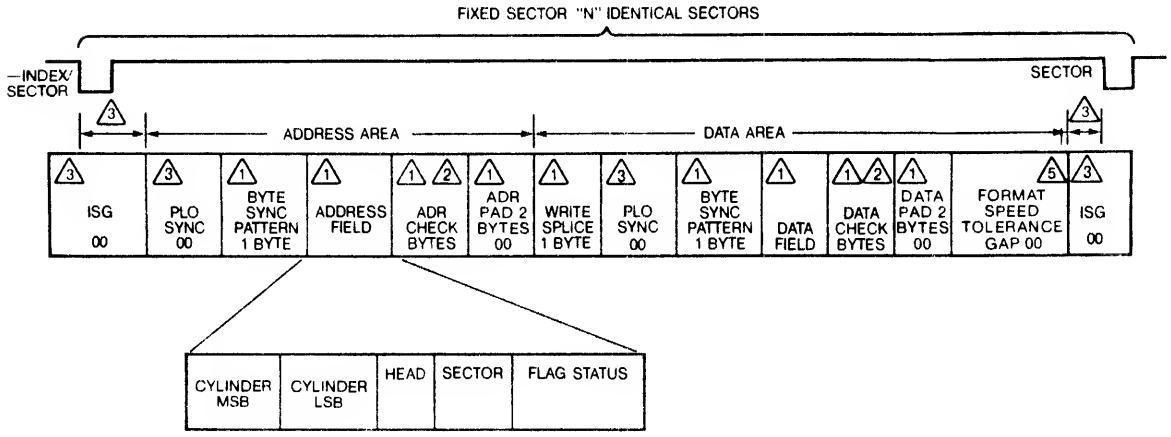
5.4.3 Fixed Sector Implementation (Controller or Drive Hard Sectored)

This section is included as an example of a fixed sector format to give meaning to the definitions given.

5.4.3.1 Format Rules (Fixed Sector)

The record format on the disk is under control of the controller. The index pulse and BYTE CLOCKS or INDEX and SECTOR pulses are available for use by the controller to indicate the beginning of a track and allow the controller to define the beginning of a sector. A suggested format for fixed data records is shown in Figure 22.

The format presented in Figure 22 consists of four functional areas; Intersector Gap, Address, Data, and Format Speed Tolerance Gap. The Data area is used to record the system's data files. The Address area is used to locate and verify the track and sector location on the Disk where the Data areas are to be recorded. This section refers to a SECTOR pulse which is generated internal to the controller from the BYTE CLOCK, or SECTOR pulses available from the drive to ease the format description.



1. THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.
2. THE NUMBER OF CHECK BYTES IS USER DEFINED.
3. PLO SYNC FIELD AND ISG ARE AS REPORTED IN RESPONSE TO THE REQUEST CONFIGURATION COMMANDS.
4. ALL BYTE NUMBERS INDICATED ARE MINIMUMS EXCEPT ADDRESS FIELD LENGTH.
5. FORMAT SPEED TOLERANCE GAP IS REQUIRED IF REFERENCE CLOCK IS NOT TIED TO ROTATIONAL SPEED. THE APPLICABILITY OF THIS GAP IS DEFINED IN THE CONFIGURATION DATA.

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FIXED SECTOR FORMAT
FIGURE 22

5.4.3.2 Intersector Gap (ISG)

The minimum Intersector Gap size is determined from the configuration data. The Intersector Gap provides a separation between each sector. The gap size is chosen to provide for:

a. Drive required write-to-read recovery time (minimum time between deassertion of WRITE GATE and assertion of READ GATE).

b. Drive required head switching time.

c. Control decision making time between sectors.

d. Other drive required ISG times.

e. Variations in detecting INDEX and SECTOR.

5.4.3.3 Address Area

The address area (Figure 22) provides a positive indication of the track and sector locations. The address area is normally read by the controller and the address bytes verified prior to a data area read or write. The address area is normally only written by the controller during a format function and thereafter only read to provide a positive indication of the sector location and establish the boundaries of the data area. The address area consists of the following bytes.

a. PLO Sync Field

These bytes are required by the drive to allow the drive's read-data phase-locked oscillator to become phase and frequency synchronized with the data bits recorded on the media. The controller should send 00's during this time.

b. Byte Sync Pattern (one byte minimum)

This byte establishes byte synchronization (i.e. the ability to partition this ensuing serial bit stream into meaningful information groupings, such as bytes) and indicates to the controller the beginning of the address field information. It is recommended that the Byte Sync Pattern contain more than a single one bit for a greater confidence level of detection.

c. Address Field

These bytes are user-defined and interpreted by the user's controller. A suggested format consists of five bytes, which allows two bytes to define the cylinder address, one byte to define the head address, one byte to define the sector address, and one byte to define flag status.

d. ADR Check Bytes - (Address Field Check Codes)

An appropriate error-detection mechanism is generated by the controller and applied to the address for file-integrity purposes. These codes are written on the media during formatting. Data integrity is maintained by the controller recalculating and verifying the address-field check codes when the address field is read. ADR check bytes are user defined.

e. ADR Pad (two bytes minimum) - (Address Field Pad)

The Address Field Pad bytes must be written by the controller and are required by the drive to ensure proper recording and recovery of the last bits of the address-field check codes. These pad bytes should be 00's

5.4.3.4 Data Area

The Data Area (Figure 22) is used to record data fields. The contents of the data fields within the Data Area are specified by the host system. The remaining parts of the Data Area are specified and interpreted by the disk controller to recover the data fields and ensure their integrity. The Data Area consists of:

a. Write Splice (one byte minimum)

This byte area is required by the drive to allow time for the write drivers to turn on and reach recording amplitude sufficient to ensure data recovery. This byte should be allowed for in the format and the controller should send 00's during this byte time.

b. PLO Sync bytes

These bytes are required when reading to allow the drive's phase-locked oscillator to become phase and frequency synchronized with the data bits recorded in the media. The controller should send 00's during these byte times.

c. Byte Sync Pattern (one byte minimum)

This byte establishes byte synchronization and indicates, to the controller, the beginning of the data field. It is recommended that this byte contain more than a single one bit.

d. Data Field

The data field contains the host system's data files.

e. Data Check Bytes - (Data-Field Check Codes)

The Data Check or Error Check Code bytes are generated by the controller and written on the media at the end of the Data Field. Data integrity is maintained by the controller recalculating and verifying the Data Field Check Codes or applying error correction algorithyms if applicable when the Data Field is read. The Data Check Field is user defined.

f. Data Pad (two bytes minimum) - (Data Field Pad)

The Data Field Pad bytes must be issued by the controller and is required by the drive to ensure proper recording and recovery of the last bits of the data field check codes. The controller should send 00's during these byte times.

5.4.3.5 Format Speed Tolerance Gap

This gap is required if bit 14 of the configuration respones flag is activated. If this gap is required, the size is determined by the controller and is:

Unformatted sector length X .01 (if configuration flag bit 11 is 0)

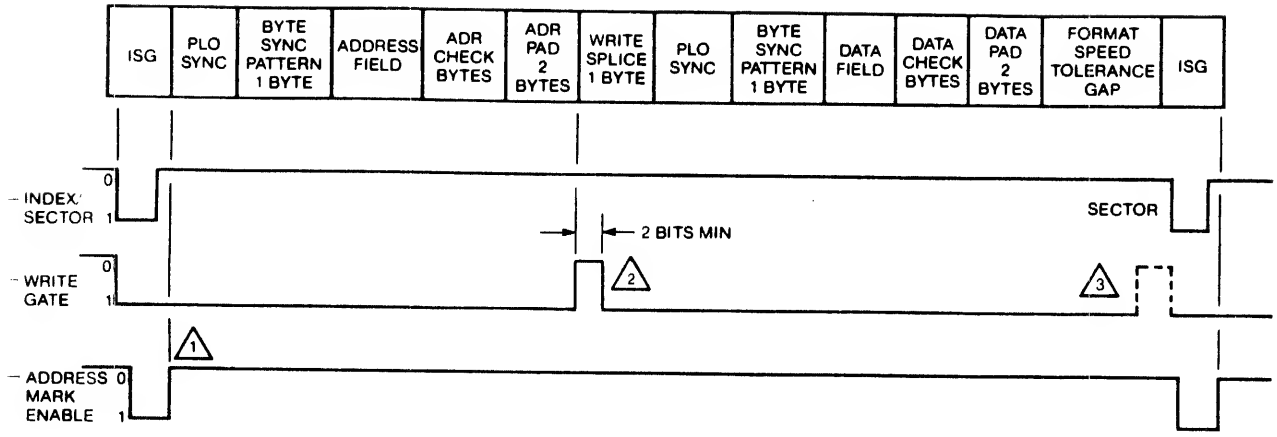
or

Unformatted sector length X .02 (if configuration flag bit 11 is 1)

This gap, if required, should be between each sector. The byte pattern in this gap should be 00's.

5.4.3.6 Fixed Sector, Address Mark, Write Gate, PLO Sync Format Timing

This timing is mainly to support drives that utilize unique encoding for PLO sync fields. The beginning of each PLO sync field must be specified by the controller. For compatability with Controller Soft Sector mode of operation, the beginning of the Header PLO Sync Field will be specified by the trailing edge of the ADDRESS MARK ENABLE signal when WRITE GATE is true. See Figure 23.



1. TRAILING EDGE OF ADDRESS MARK ENABLE SIGNIFIES THE START OF HEADER PLO SYNC FIELD. DRIVE WILL NOT WRITE AN ADDRESS MARK ON THE DISK MEDIA.
2. TRANSITION REQUIRED ONLY IF THE DISK IS READ AFTER A FORMAT AND PRIOR TO A DATA FIELD WRITE UPDATE.
3. CONTROLLER MUST REINITIALIZE TIMING WITH EACH SECTOR PULSE (NEED NOT DEACTIVATE WRITE GATE).

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FIXED SECTOR ADDRESS MARK, WRITE GATE, PLO SYNC FORMAT TIMING
FIGURE 23

5.4.4 Address Mark Implementation (Controller Soft Sectored)

This section is included as an example to give meaning to the definitions given.

5.4.4.1 Format Rules (Soft Sector)

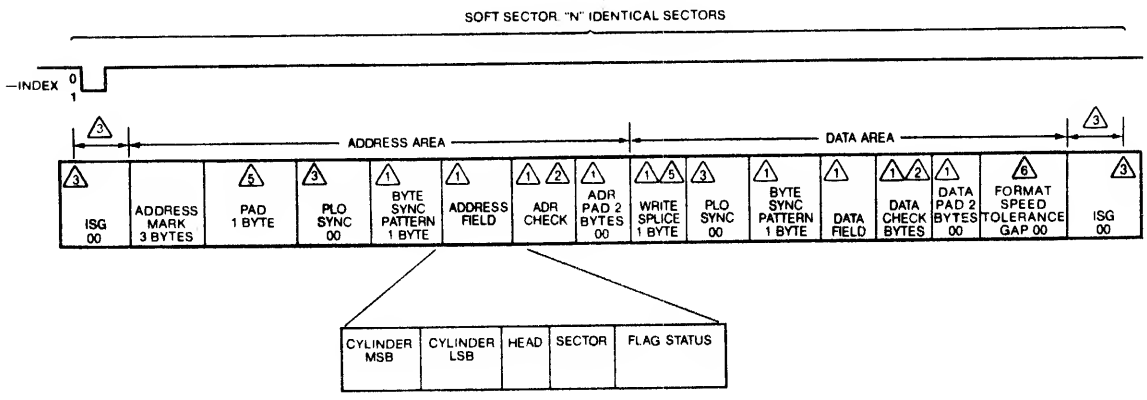
The purpose of a format is to organize a data track into smaller sequentially numbered blocks of data called sectors.

5.4.4.2 Soft Sectored Format

The format shown below in Figure 24 is similar to the format commonly used for hard sectored disk drives and indicates minimum requirements.

This format is a soft sectored type of sector which means that the beginning of each sector is defined by an ID Address Mark followed by a prewritten identification (ID) field which contains the logical sector address plus cylinder and head information. The ID field is then followed by a user supplied data field.

The definitions of the functional areas shown in the soft sectored format are identical to those described for the hard sectored format. There are some additional fields in this format and they are the Address Mark field, Address Mark Pad, and ISG speed tolerance gap.



1. THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS
2. THE NUMBER OF CHECK BYTES IS USER DEFINED.
3. PLO SYNC FIELD AND ISG ARE AS REPORTED IN RESPONSE TO THE REQUEST CONFIGURATION COMMANDS
4. ALL BYTE NUMBERS INDICATED ARE MINIMUMS EXCEPT ADDRESS FIELD LENGTH.
5. THIS AREA IS PART OF THE PLO SYNC FIELD TO ALLOW FOR READ GATE ACTIVATION DELAYS. CONTROLLER SHOULD TREAT THIS AS AN ADDITIONAL BYTE IN THE PLO SYNC FIELD
6. FORMAT SPEED TOLERANCE GAP IS REQUIRED IF REFERENCE CLOCK IS NOT TIED TO ROTATIONAL SPEED. THE APPLICABILITY OF THIS GAP IS DEFINED IN CONFIGURATION DATA

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SOFT SECTORED FORMAT
FIGURE 24

5.4.4.3 Address Mark Field

The address mark field is a field 3 bytes long and is found before the PLO sync field in the address area. The contents of this 3 byte field is drive dependent and is written by the drive when so commanded by WRITE GATE and ADDRESS MARK ENABLE active simultaneously.

Detection of Address Mark indicates the location of the beginning of a sector.

5.4.4.4 Address Mark Pad

The Address Mark Pad byte follows the Address Mark field and is to be considered a part of the PLO sync field. It's purpose is to allow for READ GATE activation delays after detecting the ADDRESS MARK FOUND signal.

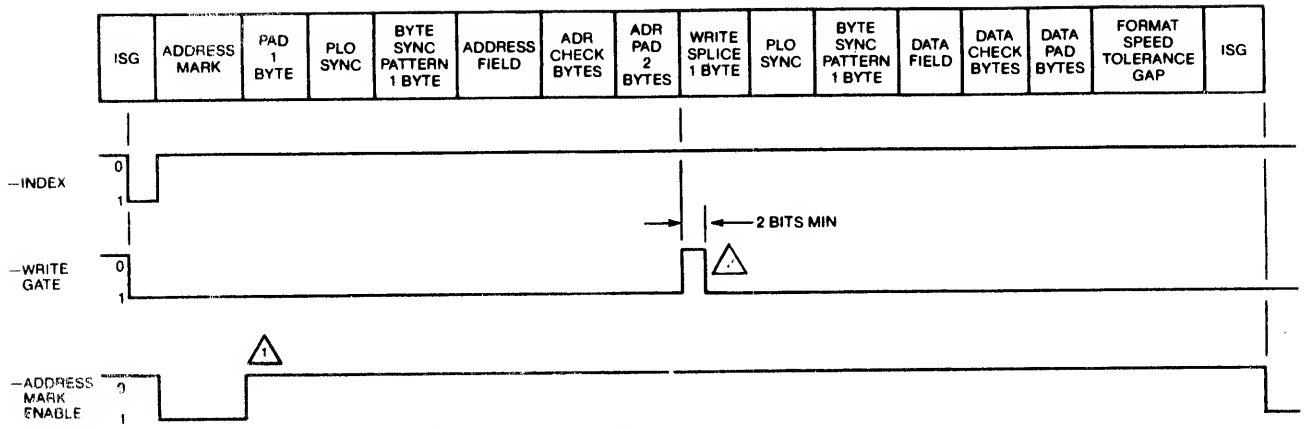
5.4.4.5 Intersector Gap (ISG) Speed Tolerance Gap

The ISG is included in the format to allow for all those items discussed in section 5.4.3.2. In addition it must also account for intersector speed tolerance.

There is also an extended ISG at the end of the track. This gap is written during a format and is used as a filler and to allow for speed tolerances. This gap must extend from the end of the last sector on the track up to the leading edge of index. The number of bytes in this gap are not included in the configuration data returned by the drive.

5.4.4.6 Soft Sectored Address Mark, Write Gate, PLO Sync Format Timing

This timing is mainly to support drives that utilize unique encoding for PLO sync fields. The beginning of each PLO sync field must be specified by the controller. The beginning of the header PLO sync field will be specified by the trailing edge of the ADDRESS MARK ENABLE signal when WRITE GATE is true. See Figure 25.



1 TRAILING EDGE OF ADDRESS MARK ENABLE SIGNIFIES THE START OF HEADER PLO SYNC FIELD.

2 TRANSITION REQUIRED ONLY IF THE DISK IS READ AFTER A FORMAT AND PRIOR TO A DATA FIELD WRITE UPDATE.

E-137-0

SOFT SECTOR ADDRESS MARK, WRITE GATE, PLO SYNC FORMAT TIMING
FIGURE 25

5.5 Defect List Option

This section describes a method of including the drives defect list on the drive. Including the defect list on the drive is optional, however, if it is to be implemented, it must be implemented as defined below.

The the defect list should reside on Sector 0 of the maximum cylinder and repeated on the maximum cylinder minus 8. This allows for redundancy should an error occur on the maximum cylinder. The sector 0 of any surface will contain the defects for that surface.
The format for the data field portion (see Figure 26) of this sector is 256 bytes with 2 bytes of CRC $(X^{16} + X^{12} + X^5 + 1)$:

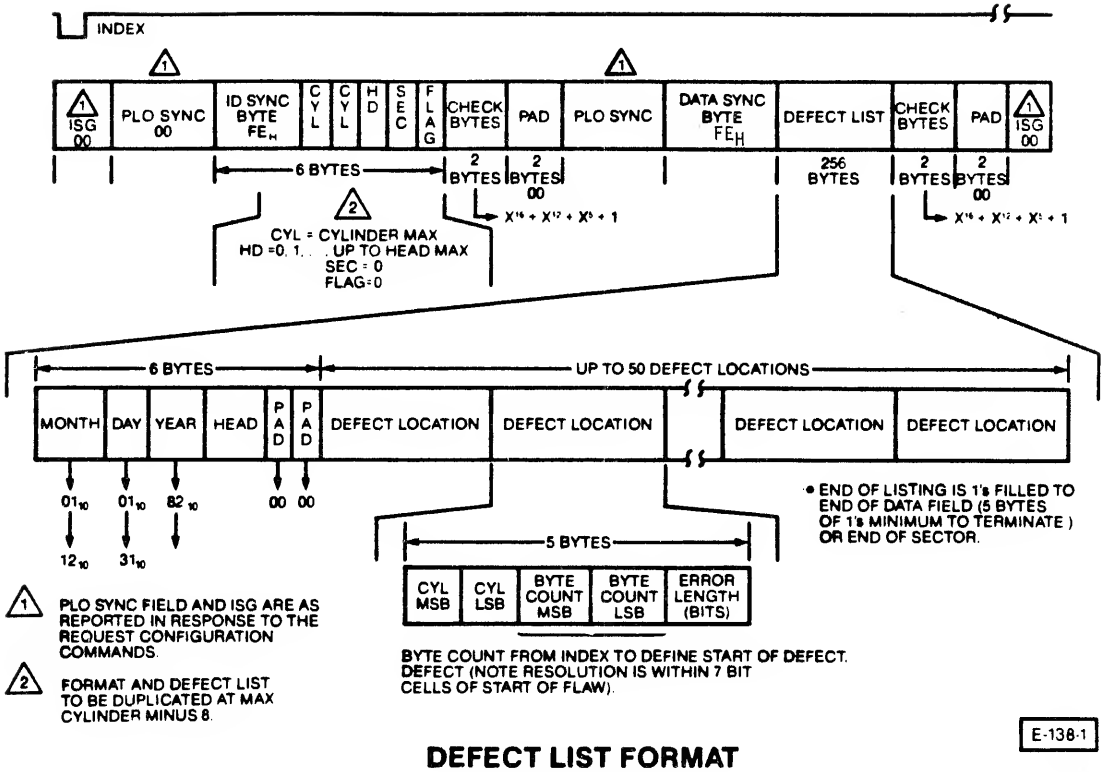
Defect locations are 5 bytes long and the bytes are defined in Figure 26.

The start of the actual defect may be off by up to 7 bits due to the one byte resolution.

The end of the defect list for each surface will be indicated by 5 bytes of ones in the defect location field or the end of the sector.

The CRC check bytes should be used if that capability exists but may be ignored if multiple reads are a more desirable approach.

Byte count is the number of Bytes from INDEX.



DEFECT LIST FORMAT
FIGURE 26

DEFECT LIST FORMAT

Figure 26

6.0 DISK DRIVE IMPLEMENTATION -- STEP MODE

This section describes the interface lines, hardware, and interface protocols necessary to implement the STEP mode version of the ESDI. Pin assignments for connectors J1 and J2 are shown in Figures 28 and 29 along with Tables 13 and 14.

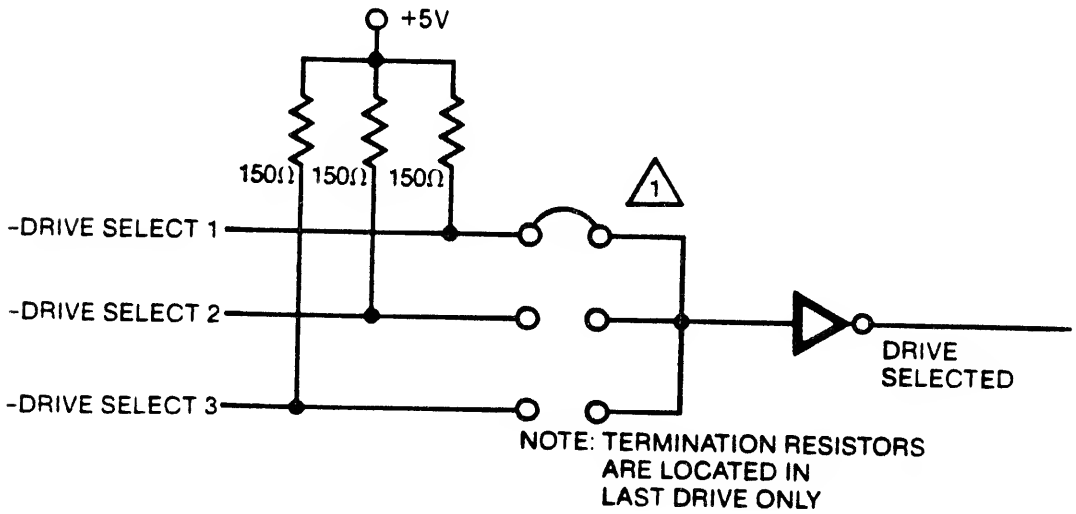
6.1 Control Input Lines

The control input signals are of two types: those to be multiplexed in a multiple drive system and those intended to do the multiplexing. The control input signals to be multiplexed are WRITE GATE, READ GATE, HEAD SELECT 2^0, HEAD SELECT 2^1, HEAD SELECT 2^2, HEAD SELECT 2^3, STEP and DIRECTION IN. The signals to do the multiplexing are DRIVE SELECT 1, DRIVE SELECT 2, and DRIVE SELECT 3.

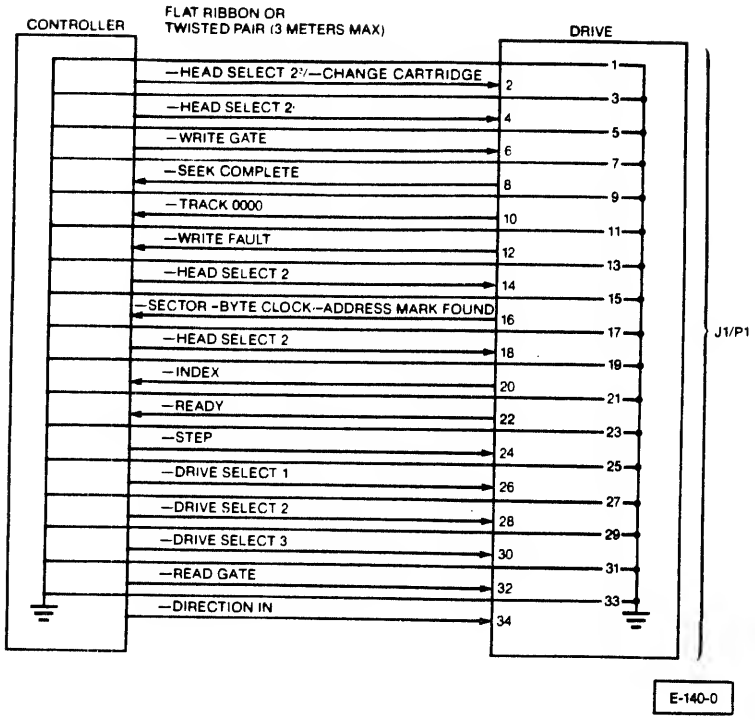
NOTE: Any lines not used should be terminated.

6.1.1 Drive Select

Any one of the DRIVE SELECT lines, when low, connects the appropriately optioned drive interface to the control lines. In this mode only 1 of 3 drives may be selected, one for each DRIVE SELECT line. See Figure 27.



DRIVE SELECT TERMINATION
FIGURE 27



E-140-0

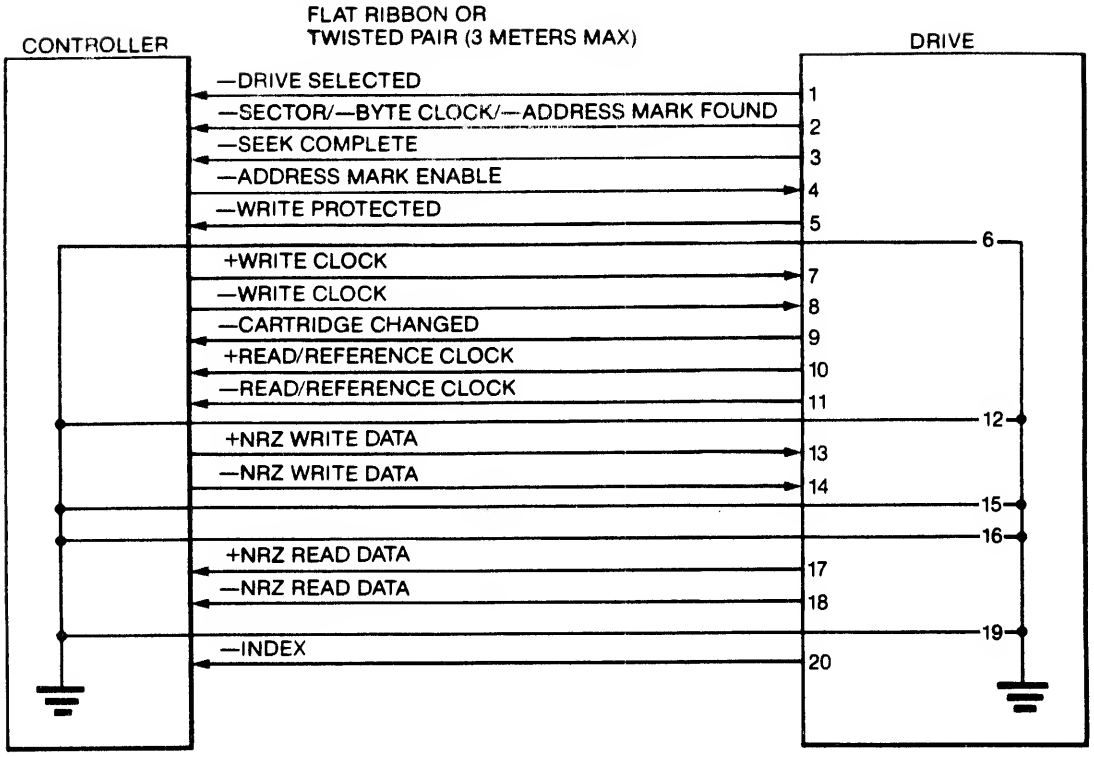
CONTROL CABLE (J1/P1) SIGNALS
(DISK IMPLEMENTATION - STEP MODE)
FIGURE 28

SIGNAL NAME	SIGNAL PIN	GROUND PIN
-HEAD SELECT 2^3/CHANGE CARTRIDGE	2	1
-HEAD SELECT 2^2	4	3
-WRITE GATE	6	5
-SEEK COMPLETE	8	7
-TRACK 0000	10	9
-WRITE FAULT	12	11
-HEAD SELECT 2^0	14	13
-SECTOR-BYTE CLOCK-ADDRESS MARK FOUND	16	15
-HEAD SELECT 2^1	18	17
-INDEX	20	19
-READY	22	21
-STEP	24	23
-DRIVE SELECT 1	26	25
-DRIVE SELECT 2	28	27
-DRIVE SELECT 3	30	29
-READ GATE	32	31
-DIRECTION IN	34	33

E-141-1

CONTROL CABLE (J1/P1) PIN ASSIGNMENTS
(DISK IMPLEMENTATION - STEP MODE)
TABLE 13

ENHANCED SMALL DEVICE INTERFACE



E-142-1

DATA CABLE (J2/P2) SIGNALS
(DISK IMPLEMENTATION - STEP MODE)
FIGURE 29

SIGNAL NAME	SIGNAL PIN	GROUND PIN
—DRIVE SELECTED	1	
—SECTOR/—BYTE CLOCK/—ADDRESS MARK FOUND	2	
—SEEK COMPLETE	3	
—ADDRESS MARK ENABLE	4	
WRITE PROTECTED	5	6
+/—WRITE CLOCK	7/8	
—CARTRIDGE CHANGED	9	
+/—READ REF CLOCK	10/11	12
+/—NRZ WRITE DATA	13/14	15/16
+/—NRZ READ DATA	17/18	19
—INDEX	20	

E-143-1

DATA CABLE (J2/P2) PIN ASSIGNMENTS
(DISK IMPLEMENTATION - STEP MODE)
TABLE 14

6.1.2 Head Select 2^0, 2^1, 2^2, and 2^3 / CHANGE CARTRIDGE

These four lines allow selection of each individual read/ write head in a binary coded sequence. HEAD SELECT 2^0 is the least significant line. Heads are numbered 0 through 15. When all HEAD SELECT lines are high (inactive), head 0 will be selected.

Head Select 2^3 has an alternate function for removeable cartridge drives. The CHANGE CARTRIDGE, when true, line causes the cartridge to spin down to allow removal.

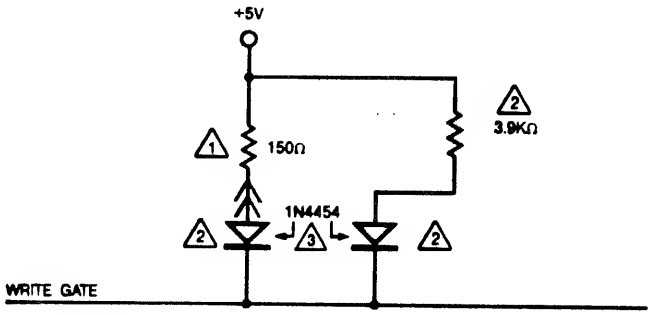
A 150 OHM resistor pack allows for line termination.

6.1.3 Write Gate

The active state of this signal, or low level, enables write data to be written on the disk.

The high to low transition of this signal creates a write splice and initiates the writing of the PLO sync field by the drive. See Figures 41 and 43. When formatting, WRITE GATE should be deactivated for 2 bit times minimum between the address area and the data area to identify to the drive the beginning of the data PLO sync field.

This line shall be protected from terminator power loss by implementation of the circuit shown in Figure 30.



1 PART OF THE TERMINATOR RESISTOR PACK IN THE LAST DRIVE OF THE DAISY CHAIN.

2 PERMANENTLY LOCATED IN THE DRIVE.

3 OR EQUIVALENT PART.

E-144-1

WRITE GATE TERMINATION
FIGURE 30

6.1.4 Read Gate

The active state of this signal, or low level, enables data to be read from the disk. This signal should be activated only during a PLO sync field and at least 11 bytes prior to the ID or Data Sync Bytes. Read gate must be deactivated when passing over a write splice area.

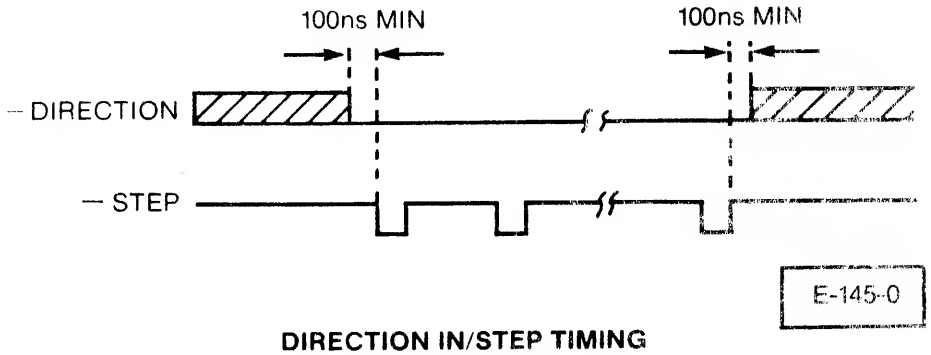
A 150 OHM resistor pack allows for line termination.

6.1.5 Direction In

The DIRECTION IN signal defines the direction of motion of the R/W heads when the STEP line is pulsed. An open circuit or high level defines the direction as "out" (or toward the lower cylinder numbers) and if a pulse is applied to the STEP line, the R/W heads will move away from the center of the disc. If this line is a low level, the direction of motion is defined as "in" and the R/W heads will move toward the center of the disc. A change in direction must meet the requirement shown in Figure 31.

A 150 OHM resistor pack allows for line termination.

NOTE: DIRECTION must not change during a sequence of step pulses.



DIRECTION IN/STEP TIMING
FIGURE 31

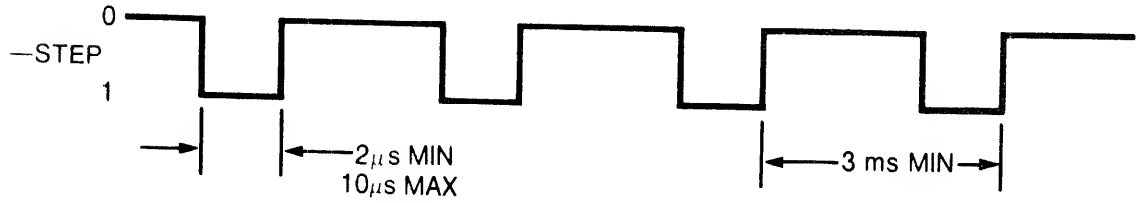
6.1.6 Step

This interface line is a control signal which causes the Read/Write heads to move in the direction of motion defined by the DIRECTION IN Line.

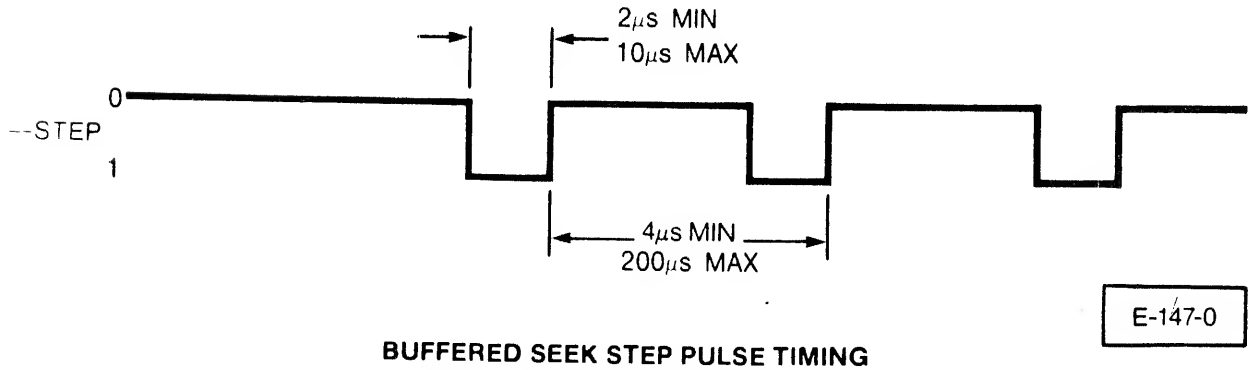
See Figure 32 for slow seek step pulse timing. Any change in the DIRECTION line must be made at least 100 nsec before the leading edge of the first step pulse. (See Figure 31).

When utilizing Buffered seeks, see Figure 33 for pulse timing.

A 150 ohm resistor pack allows for line termination.



SLOW SEEK STEP PULSE TIMING
FIGURE 32



BUFFERED SEEK STEP PULSE TIMING
FIGURE 33

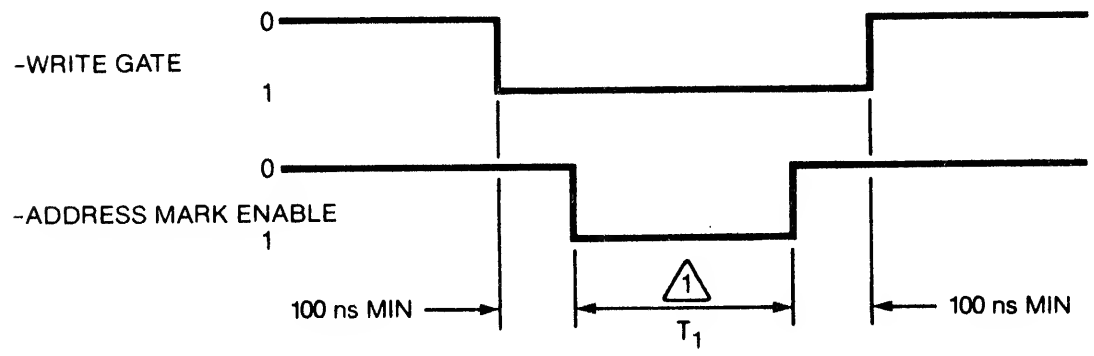
6.1.7 Address Mark Enable

This optional signal, when active with Write Gate, causes an Address Mark to be written. ADDRESS MARK ENABLE shall be active for 24 bit times. See Figure 34 for timing. The address mark written shall be left to the drive manufacturer's discretion.

ADDRESS MARK ENABLE, when active without WRITE GATE or READ GATE, causes a search for Address Marks.

If WRITE GATE is true, the LO to HI transition, or deassertion, of this signal causes the drive to begin writing the ID PLO sync field. See Figures 41 and 43.

This line must be permanently terminated in the drive. See figure 2.



E-148-0

WRITE ADDRESS MARK TIMING
FIGURE 34

6.2 Control Output Lines

The output control signals are driven with an open collector output stage capable of sinking a maximum of 48mA at low level or true state with maximum voltage of 0.4V measured at the driver. When the line driver is in the high level or false state, the driver transistor is off and collector leakage current is a maximum of 250uA.

All J1 output lines are enabled by their respective DRIVE SELECT line.

Figure 2 shows the recommended circuit.

6.2.1 Drive Selected

This status line provided is at the J2/P2 connector to inform the host system of the selection status of the drive.

The DRIVE SELECTED line is driven by a TTL open collector driver as shown in Figure 2. This signal will go active only when the drive is programmed as drive 1,2,or 3 by the drive. The DRIVE SELECT lines at J1/P1 are activated by the host system.

6.2.2 Ready

This signal indicates that the spindle is up to speed. This interface signal when true together with SEEK COMPLETE indicates that the drive is ready to read, write or seek. When the line is false, all writing and seeking is inhibited.

6.2.3 Seek Complete

This interface line indicates the status of the last seek command. This line will go to a low level or true state when the Read/Write heads have settled on the final track at the end of a seek. Reading or writing should not be attempted when SEEK COMPLETE is false.

SEEK COMPLETE will go false in the following cases:

1) A recalibration sequence is initiated (by drive logic) at power on, if the R/W heads are not over track zero.

2) 100 µsec (max) after the leading edge of a step pulse or series of step pulses.

6.2.4 Track 0000

This interface signal indicates a low level or true state only when the drive's Read/Write heads are positioned at cylinder zero (the outermost data track).

6.2.5 Write Fault

This signal is used to indicate a condition at the drive that may cause improper writing on the disk. When this line is a low level or true, further writing is inhibited at the drive until the condition is corrected.

The conditions that are detected are vendor unique.

Recommended examples of detected conditions:

a) Write current in a head without WRITE GATE active or no write current with WRITE GATE active and DRIVE SELECTED.

b) Multiple heads selected, no head selected, or improperly selected when WRITE GATE is activated.

c) Head not properly positioned over track (off-track condition detected) with write gate active.

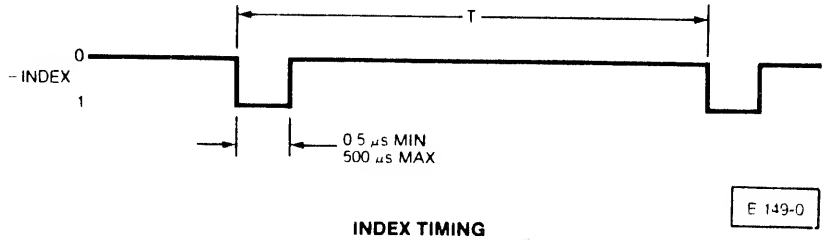
d) WRITE GATE active to a write protected drive.

e) Simultaneous activation of READ GATE and WRITE GATE.

Write fault can be reset via the interface by deselect and reselect.

6.2.6 Index

This pulse is provided by the drive once each revolution to indicate the beginning of a track. Normally, this signal is high and makes the transition to low to indicate INDEX. Only the transition at the leading edge of the pulse is accurately controlled. The period (T) of this signal is the reciprocal of the rotational speed, Figure 35. This signal is available on the command cable J1/P1 (gated) and on the data cable J2/P2 (ungated).



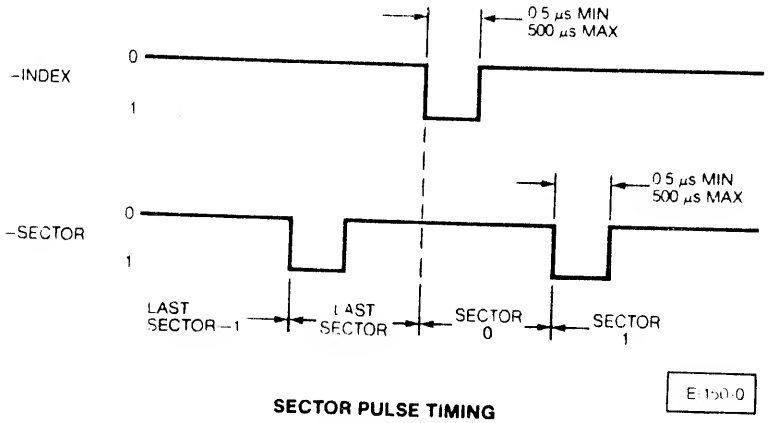
INDEX TIMING
FIGURE 35

6.2.7 Sector/Byte Clock/Address Mark Found

These three signals are mutually exclusive and therefore may share this line. The signal that is used is determined by the NRZ data transfer control implementation. These signals are available on the command cable J1/P1 (gated) and on the data cable J2/P2 (ungated). One of these three signals must be implemented by the drive manufacturer.

6.2.7.1 Sector

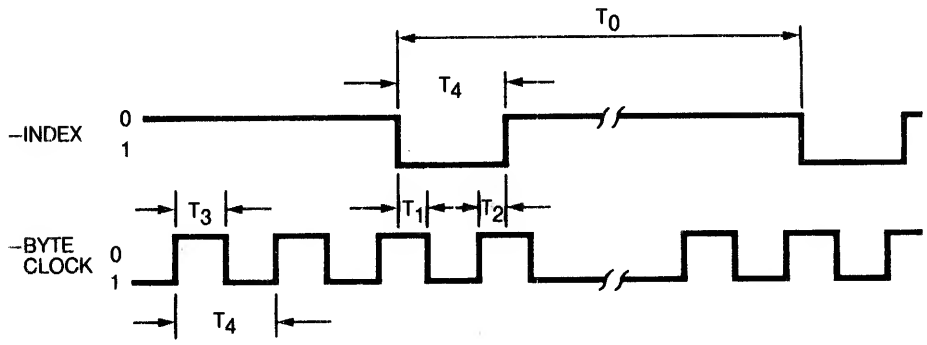
This optional interface signal indicates the presence of a sector. No short sectors are allowed. The leading edge of the sector pulses is the only edge that is accurately controlled. The index pulse indicates sector zero. See Figure 36.



SECTOR PULSE TIMING
FIGURE 36

6.2.7.2 Byte Clock

This signal occurs once per every eight Reference clock periods. This signal is provided for the controller to count the desired number of Byte Clocks to determine the sector size and beginning sector locations. The inter-relationship of INDEX and BYTE CLOCK is shown in Figure 37. This signal is continuously transmitted if the disk is up to speed and the heads are positioned over the recording zone of the disk. This clock does not have a fixed phase relationship to the recorded data.



T_0 = DISK ROTATIONAL PERIOD = INVERSE OF DISK REVOLUTIONS PER SECOND
T_1 = (0.16) x (T_4) TO (0.25) x (T_4)
T_2 = (0.25) x (T_4) TO (0.33) x (T_4)
T_3 = (0.40) x (T_4) TO (0.6) x (T_4)
T_4 = 8 TIMES THE REFERENCE CLOCK PERIOD (T)
NOTE: TIMING IS NOMINAL AND MAY VARY DUE TO SPEED VARIATIONS.

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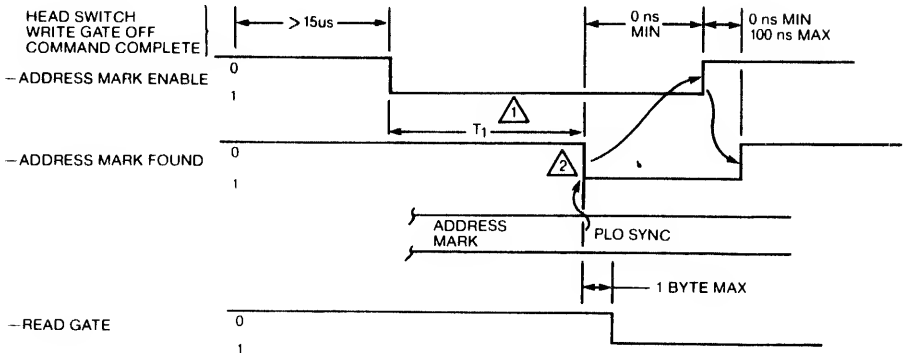
INDEX AND BYTE CLOCK RELATIONSHIP
FIGURE 37

6.2.7.3 Address Mark Found

This signal indicates that an address mark has been detected. See Figure 38 for timing.



1 T_1 24 BIT TIMES MINIMUM.

2 LEADING EDGE INDICATES THE LOCATION OF THE END OF AN ADDRESS MARK.

E-152-1

READ ADDRESS MARK TIMING
FIGURE 38

6.2.8 Write Protected

This is an optional signal. When true, it is an indication that the drive is write protected and writing should not be attempted.

6.2.9 Cartridge Changed

This is an optional signal. When true during selection, it indicates that the cartridge has been changed.

6.3 Data Transfer Lines

All lines associated with the transfer of data between the drive and the host system are differential in nature and may not be multiplexed. These lines are provided at the J2/P2 connectors on all drives.

Four pair of balanced signals are used for the transfer of data and clock :NRZ WRITE DATA , NRZ READ DATA, WRITE CLOCK, and READ/REFERENCE CLOCK. Figure 3 illustrates the recommended driver/receiver circuit.

6.3.1 NRZ Write Data

This is a differential pair that defines the data to be written on the track. This data will be clocked by the WRITE CLOCK signal. See Figure 39 for timing.

6.3.2 NRZ Read Data

The data recovered by reading a pre-recorded track is transmitted to the host system via the differential pair of NRZ READ DATA lines. This data is clocked by the READ CLOCK signal. See Figure 39 for timing. These lines must be held at a zero level until PLO sync has been obtained and data is valid.

6.3.3 Read/Reference Clock

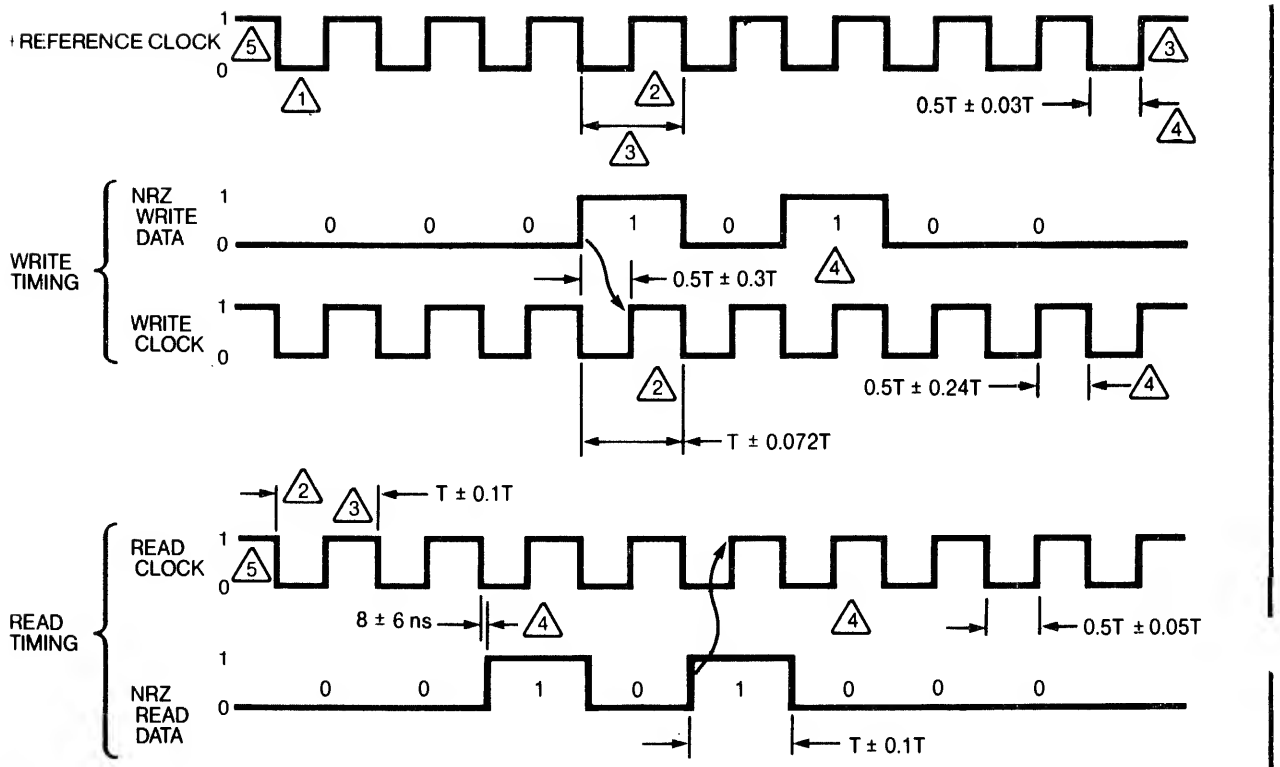
The timing diagram as shown in Figure 39 depicts the necessary sequence of events (with associated timing restrictions for proper read/write operation of the drive). Drive capabilities will determine the actual rate of data transfer range. The transitions from REFERENCE CLOCK to READ CLOCK must be performed without glitches. Two missing clock cycles are permissible.

All controllers which meet the ESDI specification must be able to operate at a minimum of 10 Mbits/second data transfer rate.

6.3.4 Write Clock

WRITE CLOCK is provided by the controller and must be at the bit data rate. This clock frequency shall be dictated by the READ/REFERENCE CLOCK during the write operation. See Figure 39 for timing.

WRITE CLOCK need not be continuously supplied to the drive. WRITE CLOCK should be supplied before beginning a write operation and should last for the duration of the write operation.



NOTES

1. ALL TIMES IN ns MEASURED AT I/O CONNECTOR OF THE DRIVE. T IS THE PERIOD OF THE CLOCK SIGNALS AND IS THE INVERSE OF THE REFERENCE OR READ CLOCK FREQUENCY.
2. SIMILAR PERIOD SYMMETRY SHALL BE IN ± 4ns BETWEEN ANY TWO ADJACENT CYCLES DURING READING OR WRITING.
3. EXCEPT DURING A HEAD CHANGE OR PLO SYNCHRONIZATION THE CLOCK VARIANCES FOR SPINDLE SPEED AND CIRCUIT TOLERANCES SHALL NOT VARY MORE THAN -5.5% to +5.0%. PHASE RELATIONSHIP BETWEEN REFERENCE CLOCK AND NRZ WRITE DATA OR WRITE CLOCK IS NOT DEFINED.
4. TIMING APPLICABLE DURING READING OR WRITING.
5. REFERENCE CLOCK IS VALID WHEN READ GATE IS INACTIVE. READ CLOCK IS VALID WHEN READ GATE IS ACTIVE AND PLO SYNCHRONIZATION HAS BEEN ESTABLISHED.
6. SEE FIGURE 3 FOR DEFINITION OF Ø AND 1 ON THESE DIFFERENTIAL SIGNAL LINES.

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NRZ READ/WRITE DATA TIMINGS
FIGURE 39

6.4 Read, Write, and Format Parameters

6.4.1 General Summary of Critical Read-Function Timing Parameters

Controller variations of the read timing are allowed if the following drive-dependent parameters are met:

a. Read Initialization Time.

A read operation may not be initiated until 15 us following a head change. Drives not able to meet 15 us must drop seek complete upon a head switch.

b. Read-Gate Timing

Requesting the drive to establish bit synchronization (i.e., enabling Read Gate) for the address area should be done no earlier than 80 $\pm$ 4 bits after the leading edge of a Sector (Index) pulse and at least 11 bytes prior to the address field sync pattern unless otherwise specified.

Read Gate may not be enabled or true during a Write Splice area (Read Gate must be deactivated one bit time minimum before a Write Splice area and may be enabled one bit time minimum after a Write Splice area.)

c. Read Propagation Delay

Data (Read) at the interface is delayed by up to 9 bit times from the data recorded on the disk media. See specific drive product specification for exact value.

d. Read Clock Timing

Read Clock and Read Data are valid within 11 bytes after Read Enable and a PLO sync field unless otherwise specified.

e. The Interface Read/Reference Clock line may contain no transitions for up to two Reference Clock periods for transitions between reference and read clocks. The transition period will also be one-half of a Reference Clock period minimum with no shortened pulse widths.

6.4.2 General Summary of Critical Write-Function Timing Parameters

Controller timing variations in the record-update function are allowed if the following drive-dependent write (and interrelated read) timing parameters are met:

a. Read-to-Write Recovery Time

Assuming head selection is stabilized, the time lapse from deactivating Read Gate to activating Write Gate shall be five Reference Clock periods minimum.

b. Write Clock-to-Write Gate Timing

Write Clocks must precede Write Gate by a minimum of two and a half Reference Clock periods.

c. Write Driver Plus Data-Encoder Turn-On From Write Gate

The write driver plus data-encoder turn-on time (write splice width) is up to 7 Reference Clock periods.

d. Write-Driver Turn-Off from Write Gate

To account for data-encoding delays, Write Gate must be held on for at least two byte times after the last bit of the information to be recorded.

e. Write-to-Read Recovery Time

The time lapse before Read Gate can be activated after deactivating the Write Gate is 10 us.

f. Head Switching Time

Write Gate must be deactivated at least 1 us before a head change.

Write Gate may not be activated until 15 us after a head change command is received by the Drive.

g. Reference Clocks Valid Time

The Read/Reference Clock lines will contain valid Reference Clocks within two Reference Clock periods after the deactivation of Read Gate. Pulse widths will not be shortened during the transition time but clock transitions may not occur for up to two Reference Clock periods.

h. Read Clocks Valid Time

The Read/Reference Clock line will contain valid Read clocks within two Clock periods after PLO synchronization is established. Pulse widths will not be shortened during this transition time, but missing clocks may occur for up to two clock periods.

i. Write Propagation Delay

Write Data Received at the I/O connector will be delayed by the Write Data Encoder by up to 8 bit times prior to being recorded on the media.

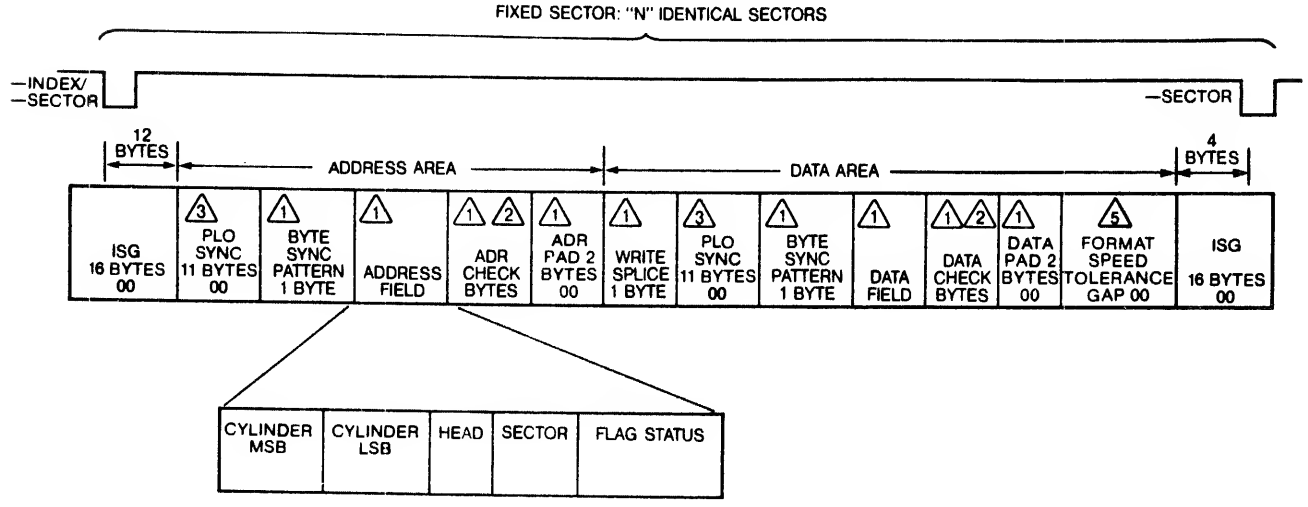
6.4.3 Fixed Sector Implementation (Controller or drive hard sectored)

This section is included as an example of a fixed sector format to give meaning to the definitions given.

6.4.3.1 Format Rules (Fixed Sector)

The record format on the disk is under control of the controller. The INDEX pulse and BYTE CLOCKS or INDEX and SECTOR pulses are available for use by the controller to indicate the beginning of a track and allow the controller to define the beginning of a sector. A suggested format for fixed length data records is shown in Figure 40.

The format presented in Figure 40 consists of three functional areas; Intersector Gap, Address and Data. The Data area is used to record the system's data files. The Address area is used to locate and verify the track and sector location on the Disk where the Data areas are to be recorded. This section refers to a SECTOR pulse which is generated internal to the controller from the BYTE CLOCK, or SECTOR pulses available from the drive to ease the format description.



(1) THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

(2) THE NUMBER OF CHECK BYTES IS USER DEFINED.

(3) PLO SYNC FIELD IS ≥ 11 BYTES.

(4) ALL BYTE NUMBERS INDICATED ARE MINIMUMS EXCEPT ADDRESS FIELD LENGTH.

(5) FORMAT SPEED TOLERANCE GAP IS REQUIRED IF REFERENCE CLOCK IS NOT TIED TO ROTATIONAL SPEED.

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FIXED SECTOR FORMAT (STEP MODE)
FIGURE 40

6.4.3.2 Intersector Gap (ISG)

The Intersector Gap is 16 bytes long and is oriented to begin four bytes before a Sector (Index) pulse and 12 bytes after a Sector (Index) pulse. This gap size was chosen for the following reasons:

a. It satisfies the drive-required write-to read recovery time (i.e., minimum time between the deactivation of Write Enable to the activation of Read Enable);

b. Drive required head switching time.

c. It allows for controller decision making time between sectors.

d. Other drive required ISG times.

6.4.3.3 Address Area

The address area (Figure 40) provides a positive indication of the track and sector locations. The address area is normally read by the controller and the address bytes verified prior to a data area read or write. The address area is normally only written by the controller during a format function and thereafter only read to provide a positive indication of the sector location and establish the boundaries of the data area. The address area consists of the following bytes.

a. PLO Sync (11 bytes minimum)

These bytes are required by the drive to allow the drive's read-data phase-locked oscillator to become phase and frequency synchronized with the data bits recorded on the media. The byte pattern sent to the drive during this time should be 00's.

b. Byte Sync Pattern (one byte minimum)

This byte establishes byte synchronization (i.e. the ability to partition this ensuing serial bit stream into meaningful information groupings, such as bytes) and indicates to the controller the beginning of the address field information. It is recommended that the Byte Sync Pattern contain more than a single one bit for a greater confidence level of detection.

c. Address Field

These bytes are user-defined and interpreted by the user's controller. A suggested format consists of five bytes, which allows one byte to define flag status bits or logical unit number, two bytes to define the cylinder address, one byte to define the head address and one byte to define the sector address.

d. ADR Check Bytes - (Address Field Check Codes)

An appropriate error-detection mechanism is generated by the controller and applied to the address for file-integrity purposes. These codes are written on the media during formatting. Data integrity is maintained by the controller recalculating and verifying the address-field check codes when the address field is read. ADR check bytes are user defined.

e. ADR Pad (two bytes minimum) - (Address Field Pad)

The Address Field Pad bytes must be written by the controller and are required by the drive to ensure proper recording and recovery of the last bits of the address-field check codes. These bytes should be 00's.

6.4.3.4 Data Area

The Data Area (Figure 40) is used to record data fields. The contents of the data fields within the Data Area are specified by the host system. The remaining parts of the Data Area are specified and interpreted by the disk controller to recover the data fields and ensure their integrity. The Data Area consists of:

a. Write Splice (one byte minimum)

This byte area is required by the drive to allow time for the write drivers to turn on and reach recording amplitude sufficient to ensure data recovery. This byte should be allowed for in the format and the controller should send 00's during this byte time.

b. PLO Sync (11 bytes minimum)

These bytes are required when reading to allow the drive's phase-locked oscillator to become phase and frequency synchronized with the data bits recorded in the media. The controller should send 00's during these byte times.

c. Byte Sync Pattern (one byte minimum)

This byte establishes byte synchronization and indicates, to the controller, the beginning of the data field. It is recommended that this byte contain more than a single one bit.

d. Data Field

The data field contains the host system's data files.

e. Data Check Bytes - (Data-Field Check Codes)

The Data Check bytes are generated by the controller and written on the media with the Data Field. Data integrity is maintained by the controller recalculating and verifying the Data Field Check Codes when the Data Field is read. Data Check Field is user defined.

f. Data Pad (two bytes minimum) - (Data Field Pad)

The Data Field Pad bytes must be issued by the controller and is required by the drive to ensure proper recording and recovery of the last bits of the data field check codes. The controller should send 00's during these byte times.

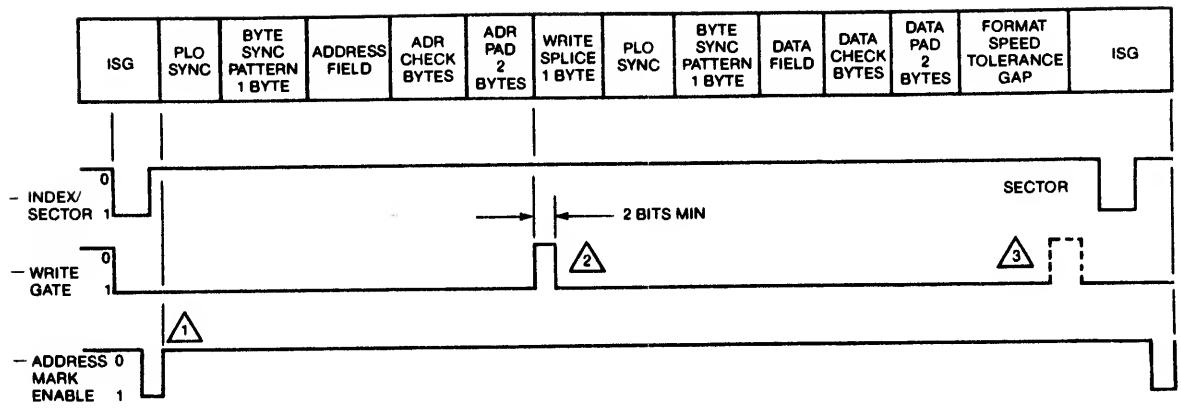
6.4.3.5 Format Speed Tolerance Gap

This gap is required in drives where the REFERENCE CLOCK is not tied to the rotational speed. The size of this gap is determined by the controller and is:

Sector length X .01 if speed tolerance of the drive is $\leq$0.5%
or
Sector length X .02 if speed tolerance of the drive is $\geq$0.5%

6.4.3.6 Fixed Sector Address Mark, Write Gate, PLO Sync Format Timing

This timing is mainly to support drives that utilize unique encoding for PLO Sync Fields. The beginning of each PLO sync field must be specified by the controller. For compatability with controllers using soft sectored mode of operation, the beginning of the header PLO Sync Field will be specified by the trailing edge of ADDRESS MARK ENABLE with WRITE GATE true. See Figure 41.



1. TRAILING EDGE OF ADDRESS MARK ENABLE SIGNIFIES THE START OF HEADER PLO SYNC FIELD. DRIVE WILL NOT WRITE AN ADDRESS MARK ON THE DISK MEDIA.
2. TRANSITION REQUIRED ONLY IF THE DISK IS READ AFTER A FORMAT AND PRIOR TO A DATA FIELD WRITE UPDATE.
3. CONTROLLER MUST REINITIALIZE TIMING WITH EACH SECTOR PULSE (NEED NOT DEACTIVATE WRITE GATE).

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FIXED SECTOR ADDRESS MARK, WRITE GATE, PLO SYNC FORMAT TIMING
FIGURE 41

6.4.4 Address Mark Implementation (Controller Soft Sectored)

This section is included as an example to give meaning to the definitions given.

6.4.4.1 Format Rules (Soft Sector)

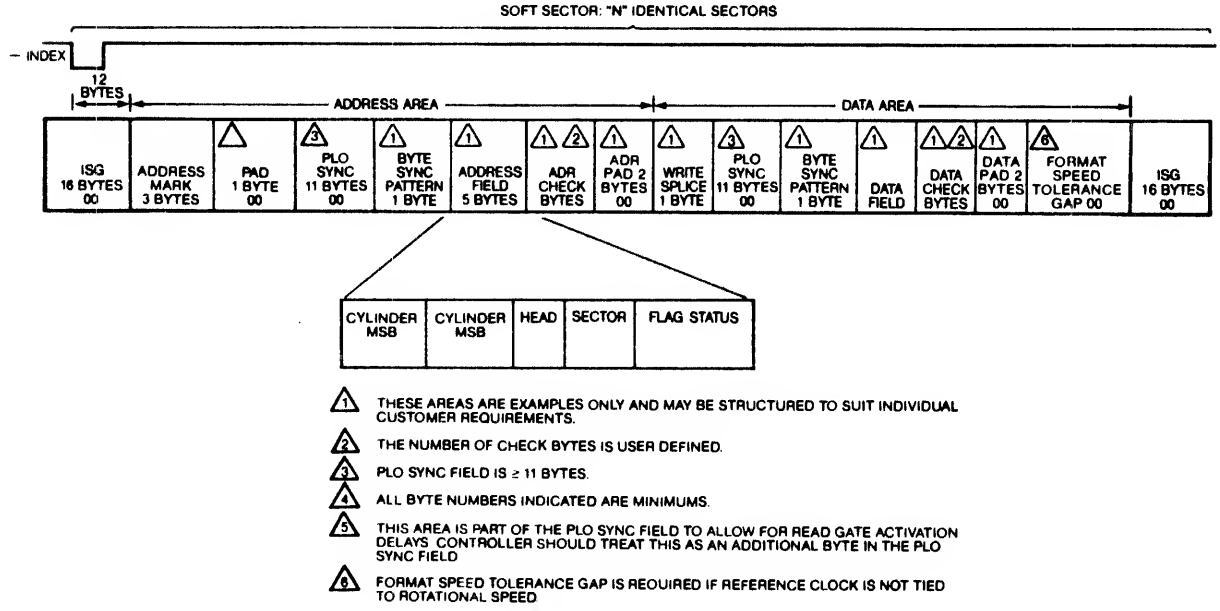
The purpose of a format is to organize a data track into smaller sequentially numbered blocks of data called sectors.

6.4.4.2 Soft Sectored Format

The format shown below in Figure 42 is similar to the format commonly used on hard sectored disk drives and indicates minimum requirements.

This format is a soft sectored type of sector which means that the beginning of each sector is defined by an Address Mark followed by a prewritten identification (ID) field which contains the logical sector address plus cylinder and head information. The ID field is then followed by a user supplied data field.

The definitions af the functional areas shown in the soft sectored format are identical to those described for the hard sectored format. There are three additional fields in this format; the Address Mark field, Address Mark pad, and ISG Speed Tolerance Gap.



SOFT SECTORED FORMAT (STEP MODE)
FIGURE 42

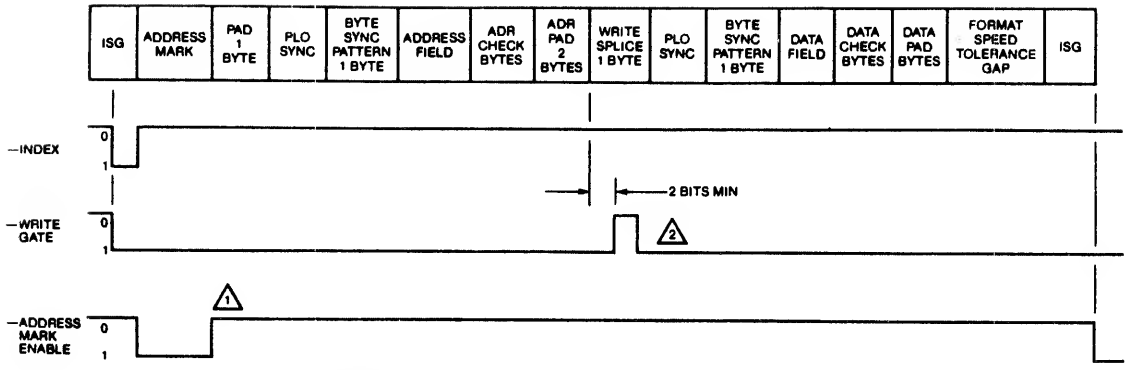
6.4.4.3 Address Mark Field

The address mark field is a field 3 bytes long and is found before the PLO sync field in the address area. The contents of this 3 byte field is drive dependent and is written by the drive when so commanded by WRITE GATE and ADDRESS MARK ENABLE active simultaneously.

Detection of Address Mark indicates the location of the beginning of a sector.

6.4.4.4 Soft Sectored Address Mark, Write Gate, PLO Sync Format Timing

This timing is mainly to support drives that utilize unique encoding for PLO Sync Fields. The beginning of each PLO sync field must be specified by the controller. The beginning of the header PLO Sync Field will be specified by the trailing edge of ADDRESS MARK ENABLE with WRITE GATE true. See Figure 43.



1 TRAILING EDGE OF ADDRESS MARK ENABLE SIGNIFIES THE START OF HEADER PLO SYNC FIELD.

2 TRANSITION REQUIRED ONLY IF THE DISK IS READ AFTER A FORMAT AND PRIOR TO A DATA FIELD WRITE UPDATE.

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SOFT SECTOR ADDRESS MARK, WRITE GATE, PLO SYNC FORMAT TIMING
FIGURE 43

6.5 Defect List Option

This section describes a method of including the drives defect list on the drive. Including the defect list on the drive is optional, however, if it is to be implemented, it must be implemented as follows:

The defect list should reside on Sector 0 of the maximum cylinder and repeated on the maximum cylinder minus 8. This allows for redundancy should an error occur on the maximum cylinder. The sector 0 of any surface will contain the defects for that surface.

The format for the data field portion (see Figure 44) of this sector is 256 bytes with 2 bytes of CRC ($X^{16} + X^{12} + X^5 + 1$):

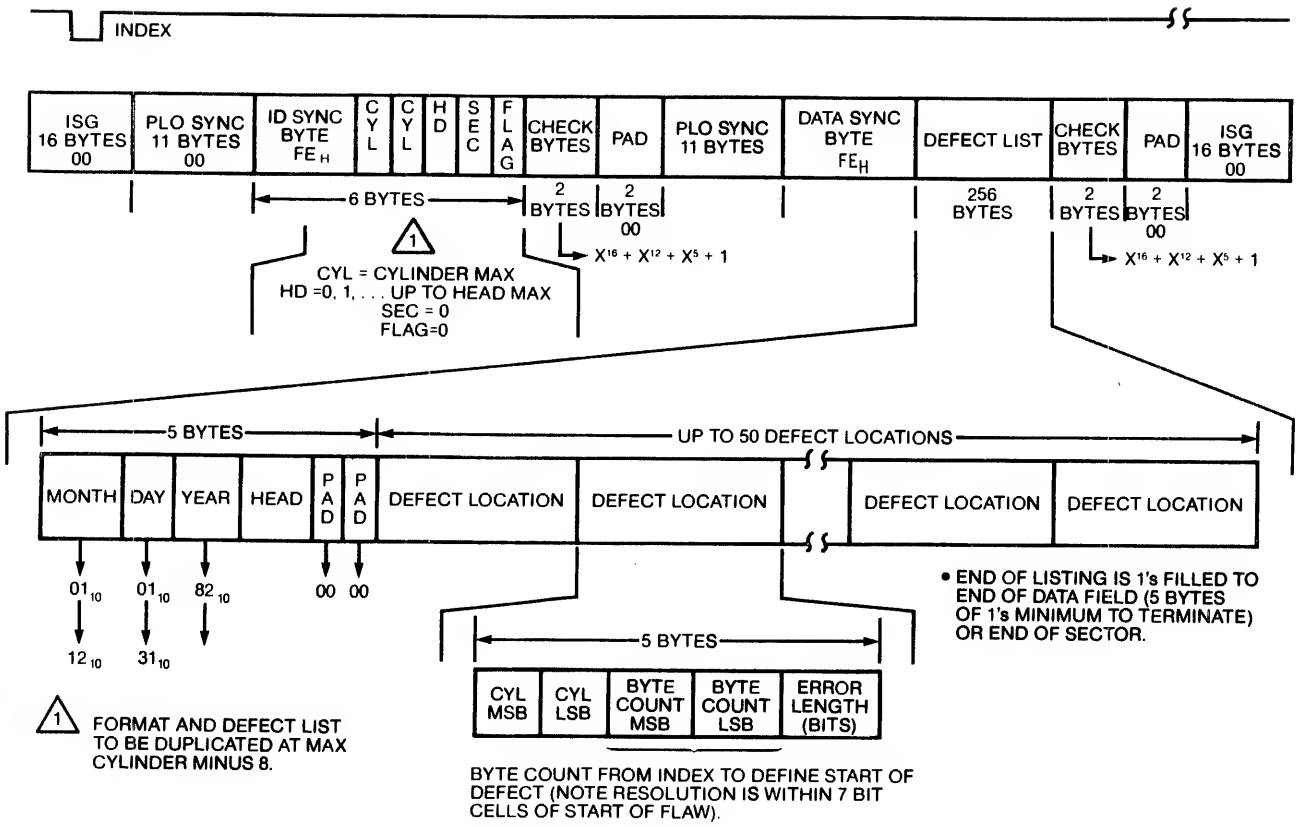
Defect locations are 5 bytes long and the bytes are defined in Figure 44.

The start of the actual defect may be off by up to 7 bits due to the one byte resolution.

The end of the defect list for each surface will be indicated by 5 bytes of ones in the defect location field or the end of the sector.

The CRC check bytes should be used if that capability exists but may be ignored if multiple reads are a more desireable approach.

Byte count is the number of bytes from INDEX.



DEFECT LIST FORMAT (STEP MODE)
FIGURE 44

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7.0 TAPE DRIVE IMPLEMENTATION - SERIAL MODE

This section describes the interface lines, hardware and interface protocols necessary to interface tape drives under the ESDI specifications. Pin assignments for connectors J1 and J2 are shown in Figures 45 and 46.

7.1 General Description

The tape drive implementation of the Enhanced Small Device Interface consists of a control cable and one or more data cables. The control cable is a daisy chained cable connecting up to seven tape or disk devices. Only the last device will have line termination for the control cable. The data cables are radially connected to the controller. The data cables utilize differential driver and receiver pairs for NRZ data and both Transmit and Receive data clocks. A write reference clock has been implemented separately from the read data clock to allow for Read after Write operation. The differential signal lines are terminated at the receiving end.

An optional block oriented tape mode has been included to provide for more efficient file structured tape access. This allows for automatic block location by the tape drive to increase efficiency of the controller operations. Controllers can request a block located on tape, then disconnect from the tape drive to service a disk drive while the tape drive locates the desired block. When the tape drive locates the requested block, it signals the controller by asserting COMMAND COMPLETE on the radial data channel. Additionally, a file mark search mode has been implemented.

This specification has been written to support both tape drives capable of Inter-Block Gap detection and those that require the controller to detect the IBG's. The controller is able to determine the capability of the tape drive with the REQUEST CONFIGURATION command. Only drives with internal IBG detection can operate with the Block locate mode.

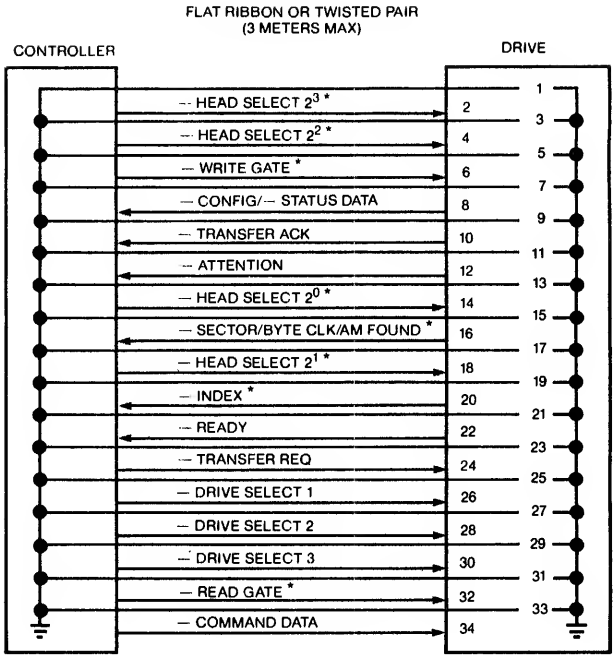
This specification provides for interfacing both non-intelligent and intelligent tape units. Both capabilities are provided for with minimal overhead to the controllers thus allowing for system flexibility while providing for cost effective systems design.

7.2 Electrical Interface

The electrical specification for tape devices is implemented as defined in Section 3.0 of this specification.

7.3 Physical Interface

The physical interface between the tape drive and the host controller is defined in Section 4.0 of this specification with the exception that more than one data cable may be used with a tape drive if the tape drive has multiple data channels. When multiple Read/Write cables are used, the first is designated J2A; additional cables would be numbered beginning with J2B. These other cables are defined as per Section 4.2.



CONTROL CABLE (J1/P1) SIGNALS
(TAPE IMPLEMENTATION)
FIGURE 45

SIGNAL NAME	SIGNAL PIN	GROUND PIN
—HEAD SELECT 2^3*	2	1
—HEAD SELECT 2^2*	4	3
—WRITE GATE*	6	5
—CONFIG/—STATUS DATA	8	7
—TRANSFER ACK	10	9
—ATTENTION	12	11
—HEAD SELECT 2^0*	14	13
—SECTOR/—BYTE CLOCK/—ADDRESS MARK FOUND*	16	15
—HEAD SELECT 2^1*	18	17
—INDEX*	20	19
—READY	22	21
—TRANSFER REQ	24	23
—DRIVE SELECT 1	26	25
—DRIVE SELECT 2	28	27
—DRIVE SELECT 3	30	29
—READ GATE*	32	31
—COMMAND DATA	34	33

* UNUSED BUT TERMINATED OR HELD FALSE
GROUND ALL ODD PINS

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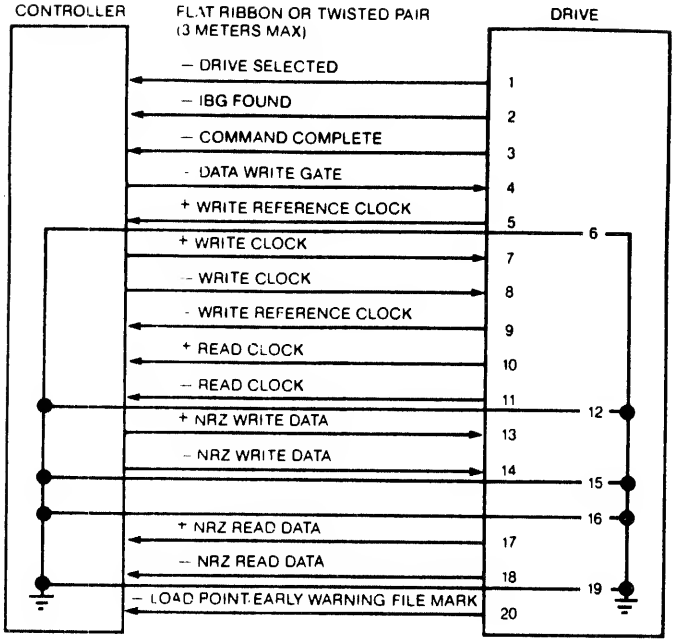
CONTROL CABLE (J1/P1) PIN ASSIGNMENTS
(TAPE IMPLEMENTATION)
TABLE 15



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GROUND PINS 6, 12, 15, 16, 19

DATA CABLE SIGNALS
J2/P2 & J5/P5 ONWOARD
(TAPE IMPLEMENTATION)
FIGURE 46

SIGNAL NAME	SIGNAL PIN	GROUND PIN
–DRIVE SELECTED	1	
–IBG FOUND	2	
–COMMAND COMPLETE	3	
–DATA WRITE GATE	4	
+WRITE REFERENCE CLOCK	5	6
+/–WRITE CLOCK	7/8	
–WRITE REFERENCE CLOCK	9	
+/–READ CLOCK	10/11	12
+/–NRZ WRITE DATA	13/14	15/16
+/–NRZ READ DATA	17/18	19
–LOAD POINT/–EARLY WARNING, –FILE MARK	20	

DATA CABLE (J2/P2) PIN ASSIGNMENTS
(TAPE IMPLEMENTATION)
TABLE 16

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7.4 Control Input Lines

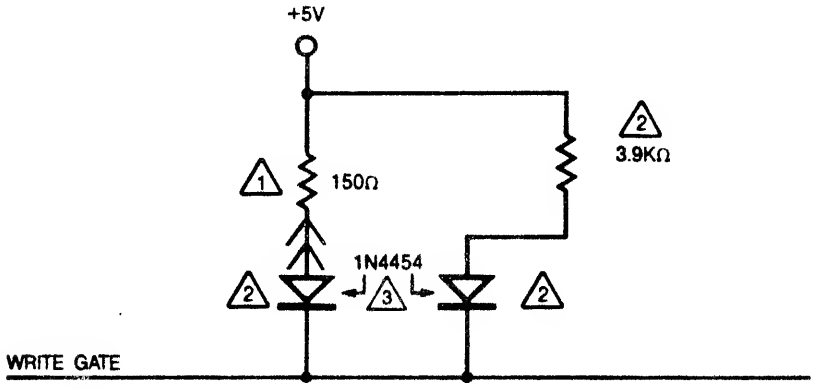
The control input signals are of two types: those to be multiplexed in a multiple drive system and those intended to do the multiplexing. The control input signals to be multiplexed are Write Gate, Read Gate, Head Select lines, Transfer Request, and Command Data. The signals to do the multiplexing are the Drive Select lines. These lines are defined for tape utilization in the following sections. Any lines not used should be terminated in the last drive as per Section 3.1 of this specification.

7.4.1 Head Selection 2^0, 2^1, 2^2, 2^3

These four lines are not used but must be terminated in the last drive.

7.4.2 Write Gate

Write Gate is not implemented on the tape drive's control cable so that simultaneous disk to tape transfers can be achieved. The effect of write gating is provided in the write command and the utilization of the Data cable's Write gate signal line described below. This allows data to be transferred to tape on the radial data channel without requiring the control channel to be logically connected to the tape transport. Hence, disk access via the control cable is possible and data may be transferred on the disk's associated data cable simultaneously. The Write Gate signal must be terminated as shown below on the control cable, Figure 47.



1. PART OF THE TERMINATOR RESISTOR PACK IN THE LAST DRIVE OF THE DAISY CHAIN.
2. PERMANENTLY LOCATED IN THE DRIVE.
3. OR EQUIVALENT PART.

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WRITE GATE TERMINATION
FIGURE 47

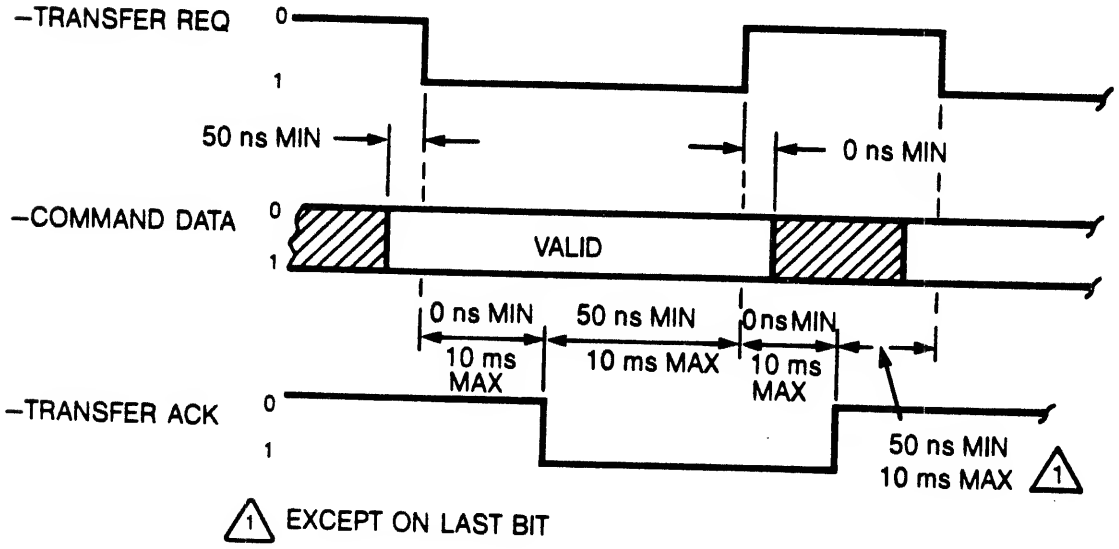
7.4.3 Read Gate

This signal line is not implemented on tape drives. This line must be terminated by the last drive.

7.4.4 Command Data

When presenting a command, sixteen (16) information bits of serial data, plus parity, will be presented on this line. (See Table 17, page 77, for the meaning of the various bit combinations.) This data is to be controlled by the handshake protocol with signals TRANSFER REQ and TRANSFER ACK. (See Figure 16, page 22 for typical serial operation.) Upon receipt of this serial data, the drive will perform the required function as specified by the bit configuration. Data is transmitted MSB first. See figure 48 below for timing.

No communication may be attempted unless the COMMAND COMPLETE line is true.



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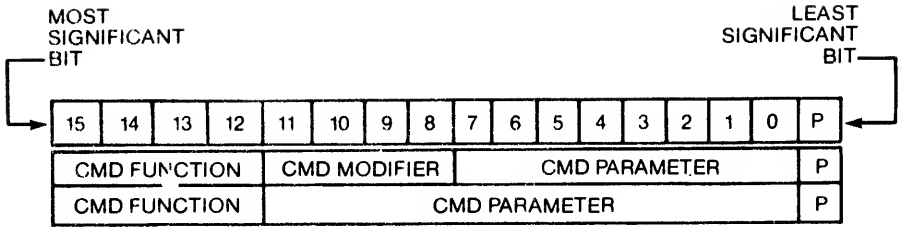
ONE BIT TRANSFER TIMING — TO DRIVE
FIGURE 48



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COMMAND DATA WORD STRUCTURE
FIGURE 49

CMD FUNCTION BIT 15 14 13 12	CMD FUNCTION DEFINITION	CMD MODIFIER APPLICABLE (BITS 11–8)	CMD PARAMETER APPLICABLE (BITS 11-0) OR (BITS 7-0)	STATUS/CONFIGURATION DATA RETURNED TO CONTROLLER
0 0 0 0	LOCATE BLOCK (OPTION)	NO	NO	NO
0 0 0 1	LOAD TAPE (OPTION)	NO	NO	NO
0 0 1 0	REQUEST STATUS	YES	NO	YES
0 0 1 1	REQUEST CONFIGURATION	YES	NO	YES
0 1 0 0	SELECT TRACK	NO	YES	NO
0 1 0 1	DECK CONTROL	YES	YES	NO
0 1 1 0	READ	YES	NO	NO
0 1 1 1	UNLOAD TAPE (OPTION)	NO	NO	NO
1 0 0 0	INITIATE DIAGNOSTICS	NO	NO	NO
1 0 0 1	SPACE FORWARD/REVERSE	YES	NO	NO
1 0 1 0	FAST POSITION EW/LP	YES	NO	NO
1 0 1 1	WRITE	YES	NO	NO
1 1 0 0	ERASE FIXED LENGTH	YES	NO	NO
1 1 0 1	HALT	NO	NO	NO
1 1 1 0	RESERVED	—	—	—
1 1 1 1	RESERVED	—	—	—

NOTES: 1. ALL UNUSED OR NOT APPLICABLE LOWER ORDER BITS MUST BE ZERO.
2. ANY "RESERVED" OR COMMAND FUNCTION RECEIVED SHALL BE TREATED AS AN INVALID COMMAND.

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COMMAND (CMD) DATA DEFINITION
(TAPE DRIVE IMPLEMENTATION)
TABLE 17

7.4.5 Command Data Bits 15 through 12 Decode Definitions

Locate Block (0000): This command causes the drive to locate a block from the beginning of the current track. Upon locating the block, the tape will be positioned in the inter-block gap preceding the addressed block in start-stop mode. COMMAND COMPLETE will be asserted upon correct execution of the LOCATE BLOCK command. The block to locate is defined by a 16 bit register internal to the deck. This register can be set by the DECK CONTROL command, and is automatically updated during a read or write command. The current block address can be read by the controller using the REQUEST CONFIGURATION command. Upon completion, COMMAND COMPLETE will be set true.

Load Tape (0001): This command will load a tape that is not normally on line. It will select Track 0 and position the tape to the LP location. Upon completion, COMMAND COMPLETE will be set true.

Request Status (0010): This command causes the drive to send 16 bits (see Table 26, page 87) of standard or vendor unique status information to the controller as determined by the command modifier bits.

Request Standard Status: When the command modifier bits 11-8 of the REQUEST STATUS command is zero (0000), the drive will respond with 16 bits of standard status. Bits 15-12 of this status are defined as state bits which do not cause ATTENTION to be asserted. Bits 11-0 of this status are fault or change of status bits that cause attention to be asserted each time one is set. See section 7.5.3.2, page 87 for response protocol and format of the status response from the drive.

Request Vendor Unique Status: When the command modifier bits 11-8 of the REQUEST STATUS command is (0001) through (1111), the drive responds with vendor unique status (undefined in this specification). The number of words available is specified by configuration data. Each word of vendor unique status is requested using a different command modifier configuration. This command modifier for the first word is 0001 and subsequent words are requested by incrementing the command modifier.

REQUEST CONFIGURATION (0011): This command causes the drive to send 16 bits (Table 25, page 86) of configuration data to the controller. The specific configuration requested is specified by bits 11-8 of the command as shown below in Table 18.

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	CONFIGURATION FLAGS
0	0	0	1	LENGHT OF TAPE (FT)
0	0	1	0	# OF DATA CHANNELS SUPPORTED
0	0	1	1	NUMBER OF TRACKS
0	1	0	0	MINIMUM BLOCK SIZE (RECOMMENDED # BYTES)
0	1	0	1	MAXIMUM BLOCK SIZE (RECOMMENDED # BYTES)
0	1	1	0	DENSITY OF RECORDING (DATA BYTES/IN)
0	1	1	1	BYTES IN IBG FIELD BITS 15-0: BYTES PER FIELD
1	0	0	0	BYTES IN PLO SYNC BITS 15-0: BYTES PER FIELD
1	0	0	1	NUMBER OF WORDS OF VENDOR UNIQUE STATUS AVAILABLE BITS 15-4: SPARE BITS 3-0: NUMBER OF VENDOR UNIQUE STATUS WORDS
1	0	1	0	CURRENT BLOCK ADDRESS (USED WITH LOCATE COMMAND)
1	0	1	1	CURRENT TRACK ADDRESS
1	1	0	0	DATA TRANSFER RATE (K BYTES/SEC)
1	1	0	1	RESERVED
1	1	1	0	RESERVED
1	1	1	1	RESERVED

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REQUEST CONFIGURATION MODIFIER BITS TABLE 18

Number of Data Channels Supported, Number of Tracks, Current Block Address and Current Track Address in Table 18 are all numbered starting from zero (e.g., track 1 equals binary 0, track 2 equals binary 1, etc.).

SELECT TRACK (0100): The select track command allows the tape drive to be conditioned to read or write a specified track. Bits 4 through 0 are significant and allow for a maximum of 32 tracks to be selected. Track selection is provided by the serial TRACK SELECT command. Addressing more tracks than available will result in a fault. Upon completion, COMMAND COMPLETE will be set true."

DECK CONTROL (0101): The deck control command is used in conjunction with the optional locate command and also to reset the interface fault and status bits. The exact function of the deck control command is defined by the command modifier bits as shown below in Table 19:

COMMAND MODIFIER BITS				FUNCTION
11	10	9	8	
0	0	0	0	RESET INTERFACE ATTENTION AND STATUS BITS 11 THROUGH 0
0	0	0	1	RESERVED
0	0	1	0	RESERVED
0	0	1	1	RESERVED
0	1	0	0	SET LOW ORDER BLOCK ADDRESS. USED WHEN LOCATE MODE IS PRESENT. BITS 7 THROUGH 0 (OPTIONAL)
0	1	0	1	SET HIGH ORDER BLOCK ADDRESS. USED WHEN LOCATE MODE IS PRESENT. BITS 7 THROUGH 0 (OPTIONAL)
0	1	1	0	SPEED AND DENSITY CHANNELS, SPEED AND DENSITY BITS 7-4: # OF DATA CHANNELS SELECTED 3-2: SPEED SELECT 1-0: DENSITY SELECT
0	1	1	1	RESERVED
1	X	X	X	RESERVED

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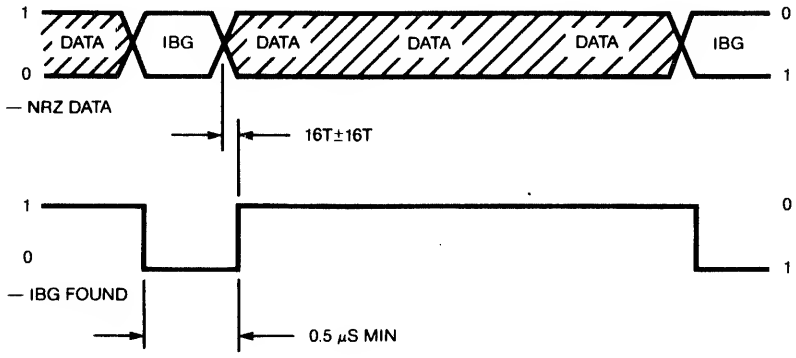
DECK CONTROL COMMAND MODIFIER BITS TABLE 19

Read (0110): The read command causes a read operation to begin at the current position on the tape. If internal deck Inter Block Gap (IBG) detection is provided, then the IBG detect signal line will go true as soon as an IBG has been detected. See Figure 50below:



READ DATA AND IBG DETECTION
FIGURE 50

Either start/stop or streaming reads are available depending on the status of the command modifier bits as shown below in Table 20. COMMAND COMPLETE is set true after the READ function is initiated, tape is up to speed and IBG FOUND is valid. The READ command is terminated by a HALT command, or other motor control command.

COMMAND MODIFIER BIT	FUNCTION
11	START/STOP OR STREAMING MODE CONTROL BIT. A HIGH CONDITION INDICATES STREAMING READ MODE. THIS BIT IS IGNORED IF ONLY ONE MODE IS PROVIDED BY THE DRIVE. INVALID COMMAND IS REPORTED WHEN THE MODE IS NOT SUPPORTED BY THE MANUFACTURER.
10	LOGICAL FORWARD/REVERSE READ. A HIGH BIT INDICATES A REVERSE READ. INVALID COMMAND REPORTED WHEN MODE IS NOT SUPPORTED BY MANUFACTURER.
9	RESERVED
8	RESERVED

READ COMMAND MODIFIER BITS
TABLE 20

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Unload Tape (0111): This command causes the drive to rewind and prepare tape for removal from the drive. Upon completion, COMMAND COMPLETE will be set true.

Initiate Diagnostics (1000): This optional command causes the drive to perform internal diagnostics. COMMAND COMPLETE indicates the completion of the diagnostics. ATTENTION with COMMAND COMPLETE indicates that a fault was encountered and STATUS should be requested to determine the cause.

Space Forward/Reverse (1001): This command causes the drive to move the tape in a logical forward or reverse direction to the next inter-block gap. The direction is set by the status of the command modifier bits as shown below in Table 21. COMMAND COMPLETE will become true after the drive has detected and stopped within the IBG.

COMMAND MODIFIER BIT	FUNCTION
11	SPACE TO FILE MARK. WHEN SET TRUE, THIS COMMAND CAUSES THE DRIVE TO POSITION THE TAPE TO THE FIRST FILE MARK IN EITHER THE LOGICAL FORWARD OR REVERSE DIRECTION AS SPECIFIED BY BIT 10. ON DRIVES NOT SUPPORTING FILE MARKS AN INVALID COMMAND WILL BE REPORTED.
10	WHEN SET FALSE THE DRIVE WILL MOVE IN A FORWARD DIRECTION. WHEN SET TRUE THE DRIVE WILL MOVE IN A REVERSE DIRECTION. AN INVALID COMMAND WILL BE REPORTED WHEN THIS FUNCTION IS NOT SUPPORTED BY THE VENDOR.
9	RESERVED
8	RESERVED

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SPACE FORWARD/REVERSE COMMAND MODIFIER BITS
TABLE 21

SPACE FORWARD/REVERSE COMMAND MODIFIER BITS

Table 21

Fast Position EW/LP (1010): This command causes the drive to move tape to the early warning or load point. Early Warning/Load Point direction is set by the status of the Command modifier bits as shown in Table 22. Upon completion, COMMAND COMPLETE will be set true.

COMMAND MODIFIER BIT	FUNCTION
11	RESERVED
10	A TRUE CAUSES TAPE TO BE MOVED TO EARLY WARNING (EW). A FALSE WILL CAUSE TAPE MOVEMENT TO LOAD POINT (LP). INVALID COMMAND REPORTED WHEN NOT SUPPORTED BY MANUFACTURER.
9-8	RESERVED

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FAST POSITON EW/LP COMMAND MODIFIER BITS
TABLE 22

Write (1011): The write command causes the deck to write data starting at the current position on tape. The "Inter-Block Gap Found" signal line will go true as soon as the tape is up to speed and the appropriate interblock gap length has been written to the tape. See Figure 51 for timing.

Either start/stop or streaming writes are available depending on the status of the command modifier bits as shown below in Table 23. COMMAND COMPLETE is set true after a WRITE command when the tape is up to speed and IBG FOUND is valid. WRITE command is terminated by a HALT Command, or other motor control command.

COMMAND MODIFIER BIT	FUNCTION
11	START/STOP OR STREAMING MODE CONTROL BIT. A HIGH CONDITION INDICATES STREAMING WRITE MODE. THIS BIT IS IGNORED IF ONLY ONE MODE IS PROVIDED BY THE DRIVE.
10	LOGICAL FORWARD/REVERSE WRITE. A LOGIC ONE INDICATES A REVERSE WRITE. INVALID COMMAND IS REPORTED WHEN THE MODE IS NOT SUPPORTED BY THE DRIVE.
9	WRITE FILE MARK MODE CONTROL BIT. A HIGH CONDITION CAUSES A FILE MARK AND AN INTERBLOCK GAP TO BE WRITTEN PRIOR TO COMMENCING THE NORMAL WRITE FUNCTION. THE INTERBLOCK GAP DETECT SIGNAL WILL GO FALSE AS SOON AS THE TAPE IS UP TO SPEED AND THE FILE MARK AND APPROPRIATE INTERBLOCK GAP LENGTH HAS BEEN WRITTEN TO THE TAPE. INVALID COMMAND WILL BE REPORTED WHEN THIS MODE IS NOT SUPPORTED BY DRIVE.
8	RESERVED

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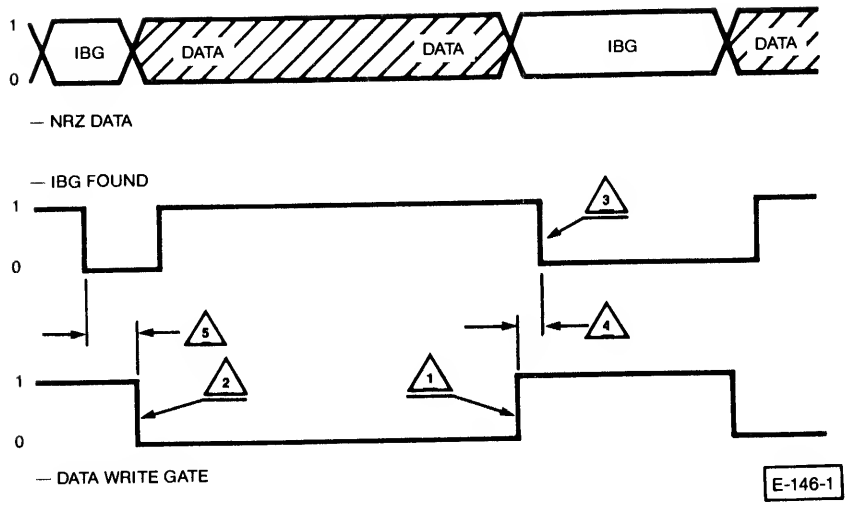
WRITE COMMAND MODIFIER BITS
TABLE 23



NOTES:
1. EDGE TRANSITION INSTALLS POST-EMBLE AND INTER-BLOCK GAP BY DRIVE WHERE SUPPORTED.
2. WRITE INITIALIZATION BY CONTROLLER.
3. EDGE INDICATES TO CONTROLLER THAT MINIMUM IBG HAS BEEN INSTALLED AND A NEW BLOCK OF DATA MAY BE WRITTEN.
4. MINIMUM MANUFACTURER SPECIFIED IBG SIZE.
5. IBG EXTENSION TIME.

WRITE DATA AND IBG TIMING
FIGURE 51

Erase Fixed Length (1100): This command causes a fixed length of tape to be erased starting at the current position. The length of tape is vendor unique. An optional length can be defined by the use of command modifier bits. Additionally, a continuous erase to End of Tape is provided for by the command modifier bits.

Continuous Erase terminates on EOT/BOT with COMMAND COMPLETE. Continuous Erase will take precedence over Fixed Length Erasures.

COMMAND MODIFIER BIT	FUNCTION
11	RESERVED
10	FORWARD/REVERSE TRUE ERASES IN THE REVERSE DIRECTION
9-8	FIXED LENGTH ERASE
	00 - 1X 01 - 2X 10 - 3X } "X" IS THE TAPE LENGTH (FT) DEFINED BY THE MANUFACTURER
	11

NOTE: DRIVES IMPLEMENTING ONLY PART OF THE ERASURE LENGTHS WILL RESPOND AS IF THE NON—SUPPORTED FIXED LENGTH ARE LEGAL.

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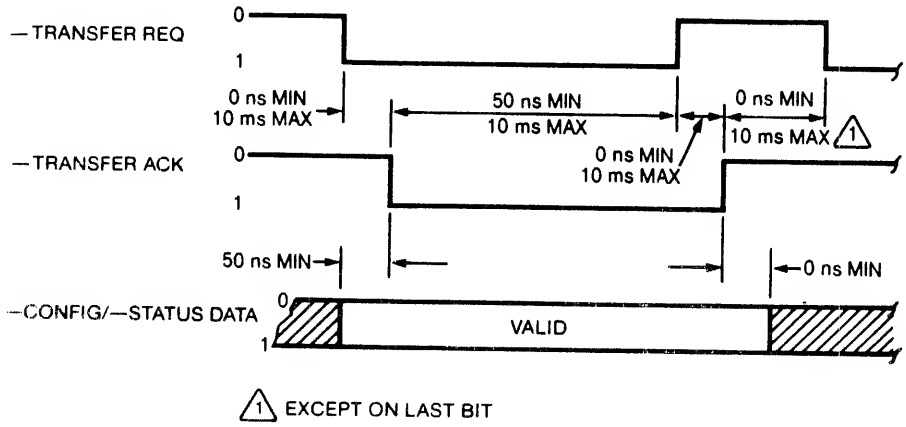
ERASE FIXED LENGTH COMMAND MODIFIER BITS
TABLE 24

HALT (1101): The HALT command will stop tape motion in and the first IBG FOUND in start/stop mode, or stop tape motion immediately in streaming mode or controller detected IBG mode when WRITE GATE is not active.

7.4.6 Transfer Request

This line functions as a handshaking signal in connection with TRANSFER ACK during command and configuration/status transfers (see Figures 48 and 52 for timing information).



ONE BIT TRANSFER TIMING — FROM DRIVE
FIGURE 52

7.4.7 Address Mark Enable

This signal is not used for tape on the control cable J1/P1 but is redefined on the data cables as Data Write Gate. The signal on J1/P1 must be terminated on the last drive.

7.4.8 Data Write Gate

This signal is a redefinition of, and replaces the disk drive function ADDRESS MARK ENABLE on the radial data cable J2/P2. Data Write Gate function is to provide timing for the writing of data onto the tape. A true condition enables the writing of data from the NRZ Write Data lines to the tape. The true to false transition installs an inter-block gap on drives with IBG detectors. This line must be permanently terminated in every drive. Refer to Figure 51 for timing information.

7.5 Control Output Lines

The output control signals are driven with an open collector output stage capable of sinking a maximum of 48 mA at low level or true state with a maximum voltage of 0.4V measured at the driver. When the line driver is in the high level or false state, the driver transistor is off and collector leakage current is a maximum of 250uA.

All J1 output lines are enabled by their respective DRIVE SELECT decodes. Refer to Figure 2, page 4 for the recommended circuit. Any lines not used should maintain a high level or false state when selected.

7.5.1 Drive Selected

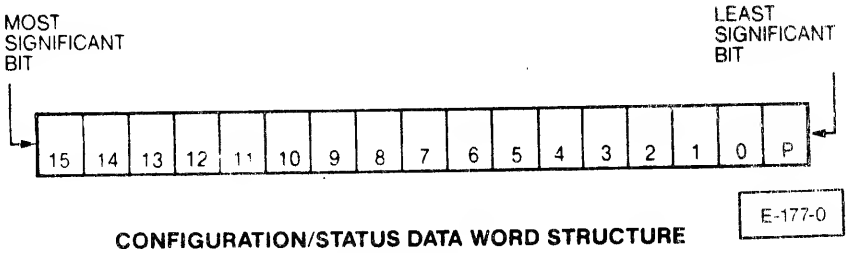
A status line provided at the J2/P2 connector to inform the host system of the selection status of the drive. The DRIVE SELECTED line is driven by a TTL open collector driver as shown in Figure 2, page 4. This signal will go active only when the drive is selected as defined in section 5.1.1, page 8. The DRIVE SELECT lines at J1/P1 are activated by the host system.

7.5.2 Ready

This signal indicates that the drive is ready to receive commands for reading, writing, and locating or any tape motion command. READY need not be true for status or configuration requests. The READY signal, when true with COMMAND COMPLETE indicates that any tape motion command is valid.

7.5.3 Configuration Status Data (Config/Status)

The drive presents serial data on this line upon request from the controller. See figure 16, page 22 for typical serial operation. This CONFIG-STATUS data will be presented to the interface and transferred using the handshake protocol with signalsTRANSFER REQUEST and TRANSFER ACKNOWLEDGE. See Figure 52, page 84. Once initiated, 16 bits plus parity will be transmitted MSB first.



CONFIGURATION/STATUS DATA WORD STRUCTURE
FIGURE 53

7.5.3.1 Configuration Response Bits

In response to the REQUEST CONFIGURATION command (see section 7.4.5, page 79), 16 bits of configuration information is returned to the controller.

BIT POSITION	FUNCTION
15	TAPE DRIVE
14	RESERVED
13	RESERVED
12	RESERVED
11	RESERVED
10	RESERVED
9	RESERVED
8	LOAD/UNLOAD SUPPORTED
7	START/STOP SUPPORTED
6	STREAMING SUPPORTED
5	FILE MARKS SUPPORTED
4	LOGICAL REVERSE READ/WRITE SUPPORTED
3	MULTIPLE SPEED SUPPORTED
2	MULTIPLE DENSITY SUPPORTED
1	LOCATE MODE SUPPORTED
0	CONTROLLER IBG DETECT REQUIRED

GENERAL CONFIGURATION RESPONSE BITS
TABLE 25

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If other command modifier bits were used, the specific configuration information shown in Table 18 (page 79) is returned for each CONFIGURATION command with those modifiers.

7.5.3.2 Status Response Bits

In response to the REQUEST STATUS command (see section 7.4.5, page 78), 16 bits of status information is returned to the controller.

Bits 15-12 of the status are defined as state bits which do not cause ATTENTION to be asserted. Bits 11-0 are fault or change of status bits that cause ATTENTION to be asserted.

BIT POSITION	FUNCTION
15	RESERVED
14	REMOVEABLE MEDIA NOT PRESENT
13	WRITE PROTECT
12	RESERVE
11	FILE MARK FOUND
10	LOAD POINT
9	EARLY WARNING
8	POWER ON RESET CONDITION EXIST (RECONFIGURATION MAY BE NEEDED)
7	COMMAND DATA PARITY FAULT
6	INTERFACE FAULT
5	INVALID OR UNIMPLEMENTED COMMAND FAULT
4	LOCATE FAULT
3	DECK FAULT
2	VENDOR UNIQUE STATUS AVAILABLE
1	* WRITE FAULT
0	REMOVEABLE MEDIA CHANGE SINCE LAST SELECTION

* Conditions that can cause WRITE FAULT include:
1. Write current in a head without a write command active.
2. Head select request while in write mode, or abnormal write command termination
3. D.C. voltages grossly out of tolerance.

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STANDARD STATUS RESPONSE BITS
TABLE 26

* Conditions that can cause WRITE FAULT include:

1. Write current in a head without a write command active.
2. Head select request while in write mode, or abnormal write command termination.

7.5.4 Transfer Acknowledge (Transfer/Ack)

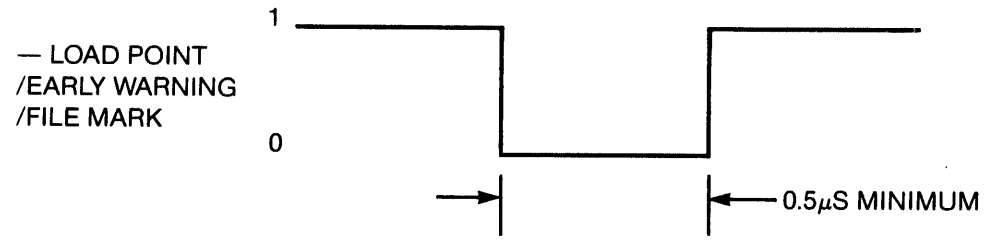
This signal functions as a handshake signal along with TRANSFER REQUEST during Command and Configuration-Status transfers. See Figure 48, page 76 and Figure 52, page 84.

7.5.5 Attention

This output line is asserted when the drive wants the controller to request its standard status. Generally, this is a result of a fault condition or a change of status. ATTENTION is cleared by the DECK CONTROL command RESET INTERFACE ATTENTION (see SECTION 7.4.5, page 79).

7.5.6 Load Point/Early Warning/File Mark

This signal renames and replaces the disk drive signal INDEX defined in Section 5.2.6, page 23. This data channel signal indicates that the tape is currently positioned at the Load Point or has passed the Early Warning mark or has found a file mark. This true condition indicates LOAD POINT, EARLY WARNING or FILE MARK and should be true upon successful completion of a LOAD command or POSITION LP/EW command or SPACE TO FILE MARK signal as shown below in Figure 54. The minimal duration of the LOAD POINT/EARLY WARNING/FILE MARK signal is shown below in Figure 54. This signal is only available on the radial data cables, and will be held at a logic false (gated) on the command cable J1/P1.



LOAD POINT/EARLY WARNING/FILE MARK TIMING
FIGURE 54

Load Point/Early Warning/File Mark Timing

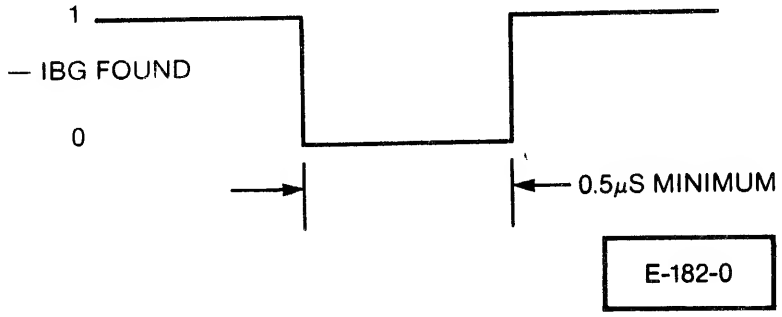
Figure 54

7.5.7 Inter-Block Gap Found (IBG Found)

This signal line replaces the SECTOR/BYTE CLOCK/ADDRESS MARK FOUND signal line on the data cables. The gated control cable signal will not be used and held at a false condition.

During a READ operation the true condition indicates an Interblock Gap has been detected by the drive. The true to false transition indicates that data has been detected and that the NRZ Read Data is valid. This transition will occur within the PLO Sync Field and can be used by the controller to begin searching for the Byte Synchronization of the Data Block.

During a WRITE Command, the False to True transition indicates the the drive has installed the minimum gap size and assertion of the Data Write Gate and Data may begin. The time between this edge and assertion of Data Write Gate is an IBG extension period. Refer to Figures 50 and 51 for Read and Write Timing. Refer to Figure 55 for Minimum Signal Timing.



INTER-BLOCK GAP TIMING
FIGURE 55

7.5.8 Command Complete

This status line is provided on the data cables as an output from the drive which allows the host to monitor the drive's COMMAND COMPLETE status during overlapped commands with other drives without selecting the drive. This signal line will go false in the following cases:

1. A LOAD command or tape load sequence is in progress on the drive, or an UNLOAD command or unload sequence is in progress on the drive.

2. Upon receipt of the first Command Data bit, COMMAND COMPLETE will go false during the entire command sequence.

3. During a power up sequence, this line will stay false until the power up sequence is complete.

This signal is driven by an open collector driver as shown in Figure 2, page 4.

Note that a WRITE and READ command will indicate command complete after the command has been initated.

7.6 Data Transfer Lines

All lines associated with the transfer of data between the drive and the host system are differential in nature and may not be multiplexed. These lines are provided at the radial data cables.

Five pairs of balanced signals are used for the transfer of data and clock: NRZ WRITE DATA, NRZ READ DATA, WRITE CLOCK, WRITE REFERENCE CLOCK and READ CLOCK. Figure 3, page 4, illustrates the recommended driver/receiver circuit.

7.6.1 NRZ Write Data

This is a differential pair that defines the data to be written on the drives associated data track for a specified data cable. This data will be clocked by the WRITE CLOCK signal. See Figure 56 for timing information.

7.6.2 NRZ Read Data

The data recovered by reading a pre-recorded track is transmitted to the host system via the differential pair of NRZ READ DATA lines. This data is clocked by the READ CLOCK signal. See Figure 56 for timing information. These lines must be held at a zero level until PLO sync has been obtained and data is valid. For systems with more than one data cable the data and clock for each may be asynchronous and have no bit or byte correlation.

7.6.3 Read Clock

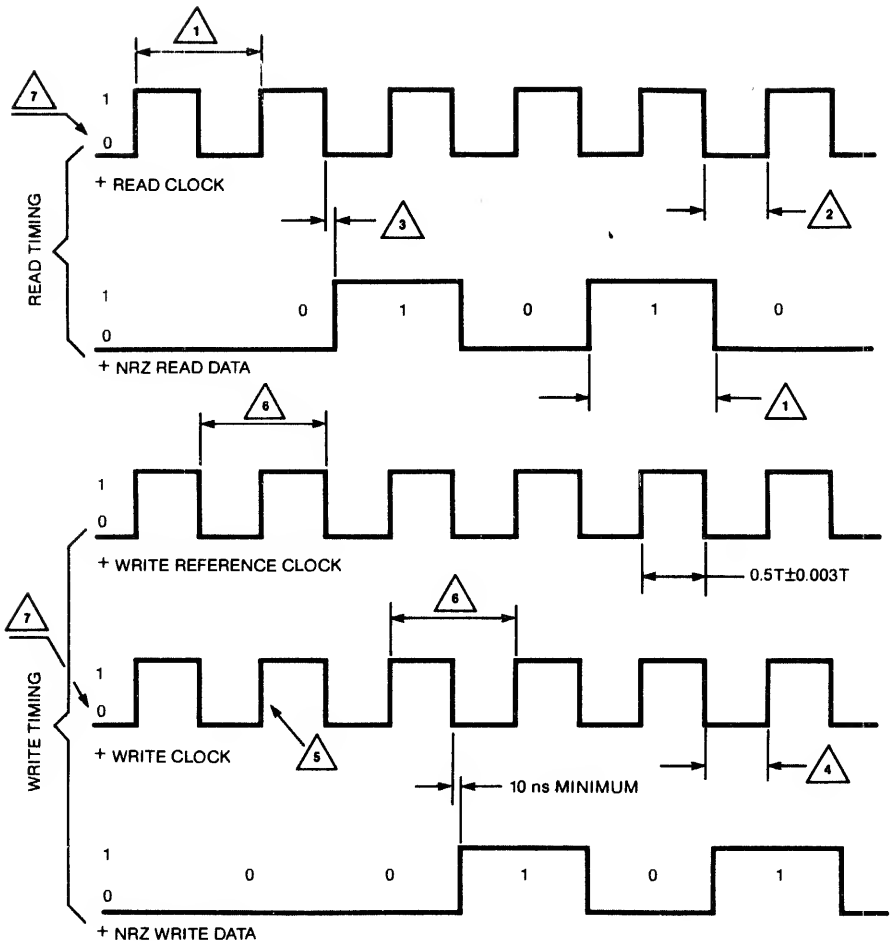
The timing diagram for READ CLOCK as shown in Figure 56 depicts the necessary sequence of events (with associated timing restrictions for proper read operations of the drive.) The READ CLOCK signal from the drive will determine the data transfer rate. READ CLOCK must be valid prior to IBG DETECT going false on a read operation. Note that the read clock is not a reference clock for write operations as the write clock has been adapted as the write reference clock for bit synchronization between the drive and the controller.

7.6.4 Write Clock

WRITE CLOCK is generated by the controller for synchronizing the transmission of data at the bit rate. Write clock is derived from Write Reference clock and need not be continuously supplied. However, it must be supplied before beginning a write operation. Note that the WRITE CLOCK is used by both the controller and the drive to determine bit synchronization and data sampling by the drive. Refer to Figure 56 for WRITE CLOCK timing information.

7.6.5 Write Reference Clock

The WRITE REFERENCE CLOCK signal from the drive will determine the data transfer rate. This clock is used by the controller to synchronize the NRZ WRITE DATA and WRITE CLOCK signals.



NOTES:

1. T ±0.25T — ALL TIMES IN NS MEASURED AT I/O CONNECTOR OF DRIVE.
2. 0.5T ±0.25T — TIMING APPLICABLE DURING READING.
3. 0.0 ±50NS DURING READING.
4. 0.5T ±0.03T — TIMING APPLICABLE DURING WRITING.
5. SAMPLING EDGE BY DRIVE.
6. DURING WRITING OF DATA CLOCK VARIANCE WILL NOT EXCEED ±5.5% PHASE RELATIONSHIP BETWEEN WRITE REFERENCE AND WRITE CLOCK OR WRITE CLOCK IS UNDEFINED.
7. READ CLOCK AND WRITE REFERENCE CLOCK MAY BE HELD LOW DURING READING OR WRITING OF DATA FOR A MAXIMUM OF 32 CLOCK PERIODS FOR SYNCHRONIZATION OF DRIVE ELECTRONICS.

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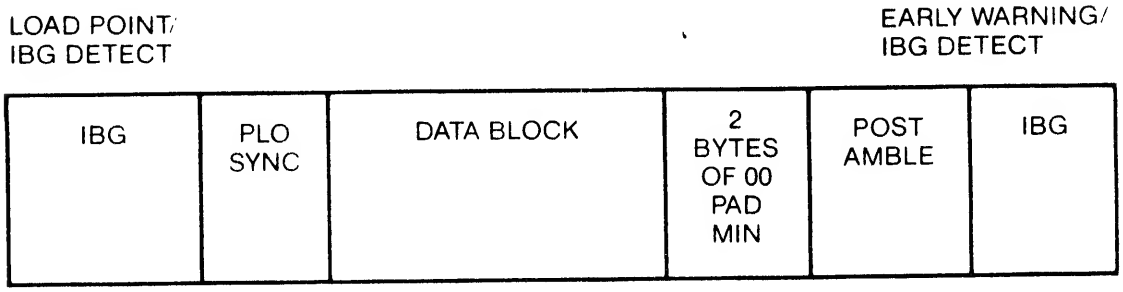
NRZ READ/WRITE DATA TIMINGS
FIGURE 56

7.7 Format Rules

The block format on the tape is under control of the controller. The IBG DETECT and LOAD POINT signals are available for use by the controller to indicate the beginning of tape and the beginning of a valid block to read or write. A minimal requirement of tape formatting is given as follows:



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REQUIRED BASE FORMAT
FIGURE 57

Where the IBG format can be either a blank segment of tape or a predefined format determined by the manufacturer and readable by the controller using the REQUEST CONFIGURATION command. The drive must detect the Inter-Block Gaps and control the IBG DETECT line as specified in Figure 50, 51 and 55 for deck control.

The PLO Sync fields and the postamble fields are direct bit order reversals of one another. That is, the PLO Sync field is manufacturer defined and readable by the controller by the REQUEST CONFIGURATION command. The postamble is the reversed bit sequence of the PLO Sync field and will be written by the drive. This allows for forward or reverse reading of data on a tape. The controller should send 00's during the PLO Sync field and a minimum of 2 bytes of 00's as pad characters. Drives only supporting forward Read and Write need not supply the postamble.

The 2 bytes of 00 PAD are not needed if the optional POST AMBLE is used for reserve read operations. If the optional POST AMBLE is not used then the 2 bytes of PAD are required in the format.

- END OF ESDI SPECIFICATION -